GAMMA-11

GAMMA 11 SYSTEM
INSTALLATION AND
MAINTENANCE MANUAL

EP-GM11A-TM-001

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FICHE 1 OF 1

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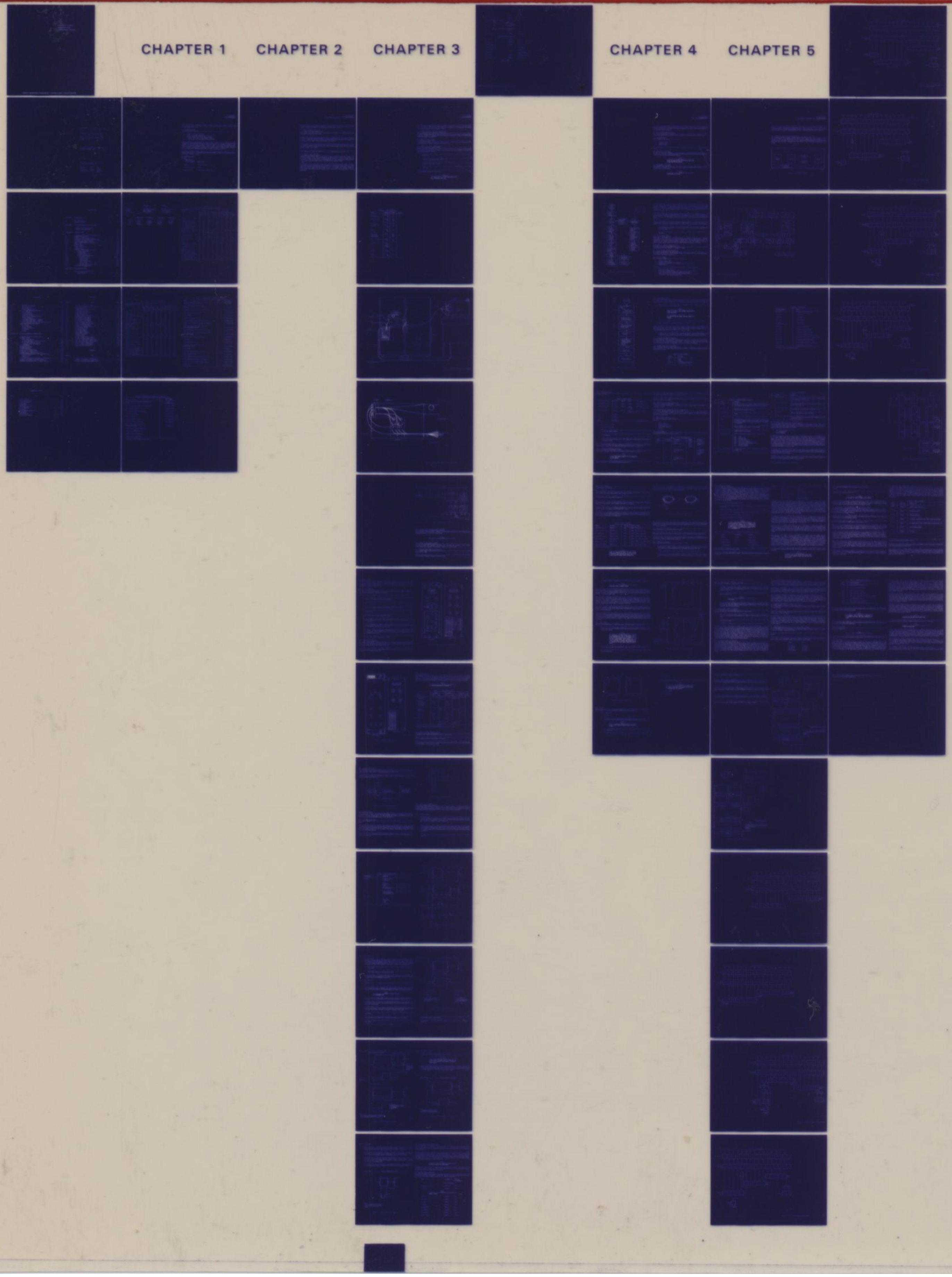
MADE IN USA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CHAPTER 4
CHAPTER 5

Gamma-11 system installation and maintenance manual

EK-GM11A-TM-001

digital equipment corporation • marlborough, massachusetts

1st Edition, April 1978

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CHAPTER 1

CHAPTER 1
DESCRIPTION

The Gamma-11 System is designed to be used in hospitals to acquire, store, process and display data from a Gamma Camera. The Gamma Camera records the distribution of a radioactive isotope that has been entered into a patient.

1.1 CONFIGURATION

The Gamma-11 system described in this manual includes the following major subsystems.

1. A PDP-11/34 Central Processor
2. An NC11-A Camera Interface for a Gamma Camera
3. RK05 or RK06 Dual Disk Storage Subsystem
4. A VSV01 Color Video Graphics Display Subsystem
5. An LA36 DECwriter II Keyboard Printer Terminal

These subsystems are configured with two types of memory: magnetic core or MOS (metal oxide semiconductor). The Gamma-11 software provides a single job (SJ) or foreground/background (FB) capability. For quick-reference, the major components, options, and assemblies included in each Gamma-11 configuration are listed in Table 1-1 and 1-2. Table 1-1 lists the items included in the PDP-11/34 core memory configurations, while Table 1-2 includes the PDP-11/34 MOS systems. Hardware manuals and documents relating to the Gamma-11 system are listed in Table 1-3.

The hardware differences between single-job (SJ) and foreground/background (FB) systems are the addition of 16K of memory, VT52 DECscope Terminal, and AR11 required for F/B software systems, as indicated in Tables 1-1 and 1-2.

1.2 SPECIFICATIONS

Electrical

Voltage Range	
115 Vac Nominal	104–127 Vac
230 Vac Nominal	208–254 Vac
Frequency	50 Hz or 60 Hz ± 0.5 Hz
Power Consumption	3.0 kVA
Heat Dissipation	2520 kg·cal/h (10,000 BTU/hr)

Environmental

	Operating	Storage
Temperature	10° - 32° C (50° - 90° F)	-40° - 66° C (-40° - 151° F)
Humidity	20%-80%; no condensation	20%-80%; no condensation
Altitude	2.4 km (8000 ft)	3.5 km (10,000 ft)
Rate of Change	5.5° C/h (10° F/h)	5.5° C/h (10° F/h)

Physical

	Height cm (in)	Width cm (in)	Depth cm (in)	Weight kg (lb)
VRV01	47 (18.5)	4.83 (19)	28.5 (11.2)	22.7 (50)
LA36	85 (33.5)	69.8 (27.5)	60.7 (24)	46.4 (102)
VT52	36 (14.1)	53 (21.9)	69 (27.2)	20 (44)
H967	128 (50)	56 (22)	76 (30)	

Table 1-1 GAMMA-11 Core Memory Configurations

Hardware Components, Options and Assemblies	Single Job		Foreground/Background					
	-NA 115 V 60 Hz	-NB 230 V 50 Hz	-NC 115 V 60 Hz	-ND 230 V 50 Hz	-PA 115 V 60 Hz	-PB 230 V 50 Hz	-PC 115 V 60 Hz	-PD 230 V 50 Hz
PDP-11/34A Central Processor	-HF	-HF	-HF	-HF	-LF	-NB	-LF	-ND
includes								
KD11-EA Processor	1	1	1	1	1	1	1	1
MM11-DP Core Memory (16K)	1	1	1	1	1	1	1	1
DL11 Serial Line Asynchronous	-WA	-WA	-WA	-WA	-WA	-WA	-WA	-WA
BA11-K Mounting Box (10.5)	1	1	1	1	1	1	1	1
KY11-LB Programmable Console	1	1	1	1	1	1	1	1
M7850 Parity Control	1	1	1	1	1	1	1	1
M9301-YB Bootstrap Terminator	1	1	1	1	1	1	1	1
RK11D Disk Drive Controller	1	1	1	1	1	1	1	1
RK05J Disk Drive (2.5 M Byte Disk)	-AA(2)	-BB(2)	-AA	-BB	-AA(2)	-AB(2)	-AA	-AB
RK05F Disk Drive (5.0 M Byte Disk)	-	-	-FA	-FD	-	-	-FA	-FD
H967 Short Cabinet								
includes								
861 Power Controller	-C	-B	-C	-B	-C	-B	-C	-B
LA36 DECwriter II Keyboard Printer Terminal	-CE	-CJ	-CE	-CJ	-CE	-CJ	-CE	-CJ
NC11 Camera Interface	-AA	-AB	-AA	-AB	-AA	-AB	-AA	-AB
VSV01 Color Video Graphics Display Subsystem	-BA	-BB	-BA	-BB	-BA	-BB	-BA	-BB
includes								
VTV01 Color Video Controller	1	1	1	1	1	1	1	1
VRV01 Color Video Monitor	1	1	1	1	1	1	1	1
CU5-B Camera	1	1	1	1	1	1	1	1
KW11-P Programmable Real-Time Clock	1	1	1	1	1	1	1	1
M9202 Unibus Connector	1	1	1	1	1	1	1	1
MM11-DP Core Memory (16K)	-	-	-	-	1	1	1	1
BA11 Expansion Mounting Box					-LF	-LF	-LE	-LF
DD11-CK Backpanel Mounting Unit					1	1	1	1
AR11-KT Analog Real-Time Subsystem					1	1	1	1
70-11765-15 Joystick Cable					1	1	1	1
VT52 DECscope Display Terminal					-AA	-AB	-AA	-AB
DL11-WA Serial Line Asynchronous					1	1	1	1

Table 1-2 GAMMA-11 MOS Memory Configuration

Hardware Components, Options and Assemblies	Single Job		Foreground/Background					
	-NE 115 V 60 Hz	-NF 230 V 50 Hz	-PE 115 V 60 Hz	-PF 230 V 50 Hz	-PJ 115 V 50 Hz	-PK 115 V 60 Hz	-PL 230 V 50 Hz	-PN 115 V 50 Hz
PDP-11/34A Central Processor	-DE	-DF	-LE	-LF	-LE	-LE	-LF	-LF
includes								
KD11-EA Processor	1	1	1	1	1	1	1	1
MS11-JP MOS Memory (16K)	1	1	2	2	2	2	2	2
DL11-WA Serial Line Asynchronous Interface	1	1	1	1	1	1	1	1
BA11-K Mounting Box	1	1	1	1	1	1	1	1
KY11-LB Programmer's Console	1	1	1	1	1	1	1	1
M7850 Parity Control	1	1	1	1	1	1	1	1
M9301-YB Bootstrap Terminator	1	1	1	1	1	1	1	1
RK11D Disk Drive Controller	1	1	1	1	1			
RK05J Disk Drive	-AA(2)	-AB(2)	-AA(2)	-BB(2)	-BB(2)			
RK05F Disk Drive	-	-	-	-				
RK611 Controller						1	1	1
RK06 Single Access Disk Drive						-EA	-ED	-EC
H967 Short Cabinet	2	2	2	2	2	1	1	1
includes								
861 Power Controller		-B	-C	-B	-C	-C	-B	-C
LA36 DECwriter II Keyboard Printer Terminal	-CE	-CJ	-CE	-CJ	-CH	-CE	-CJ	-CH
NC11 Camera Interface	-AA	-AB	-AA	-AB	-AA	-AA	-AB	-AA
VSV01 Color Video Graphics Display Subsystem	-BA	-BB	-BA	-BB	-BA	-BA	-BB	-BA
includes								
VTV01 Color Video Controller	1	1	1	1	1	1	1	1
VRV01 Color Video Monitor	1	1	1	1	1	1	1	1
CU5-B Camera	1	1	1	1	1	1	1	1
KW11-P Programmable Real-Time Clock	1	1	1	1	1	1	1	1
M9202 Unibus Connector Jumper	1	1	1	1	1	1	1	1
BA11-L Extension Mounting Box			1	1		1	1	1
DD11-CK Backpanel Mounting Unit			1	1				
AR11-KT Analog Real-Time Subsystem			1	1	1	1	1	1
70-11765-15 Joystick Cable			1	1	1	1	1	1
VT52 DECscope Display Terminal			-AA	-AB	-AC	-AA	-AB	-AC
DL11-WA Serial Line Asynchronous			1	1	1	1	1	1

Table 1-3 Related Hardware Manuals and Documents

Title	Part Number
PDP-11/34 System User's Manual	EK-11034-OP
PDP11 Field Installation and Acceptance Procedure	EK-FS003-IN
KD11-E Central Processor Maintenance Manual	EK-KD11E-TM
BA11-K Mounting Box Manual	EK-BA11K-MM
BA11-K IPB	EK-BA11K-IP
BA11-L Mounting Box Manual	EK-BA11L-MM
MS11-E-J MOS Memory Maintenance Manual	EK-MS11E-MM
MM11-D, DP Core Memory Maintenance Manual	EK-MM11D-TM
DL11-W Serial Line Unit/Real-TIme Clock Option Maintenance Manual	EK-DL11W-MM
M9301 Bootstrap Terminator Maintenance Manual	EK-M9301-MM
RK11-D AND RK11-E Moving Head Disk Drive Controller Manual	EK-RK11D-MM
RK05 Disk Drive Maintenance Manual	EK-0RK05-MM
RK05 IPB	EK-0RK05-IP
RK05/RK05J PM Procedure	EK-RK05J-PM
861-A, B, C, D, E, F Power Controller Maintenance Manual	EK-861AB-MM
861-A-F IPB	EK-861-IP
LA36 DECwriter II Maintenance Manual	EK-0LA36-MM
LA36 DECwriter II IPB	EK-0LA36-IP
RK611/RK06 Disk Subsystem Installation Manual	EK-RK611-IM
RK611/RK06 Disk Subsystem Users Manual	EK-RK611-OP
VSV01 Color Video Graphics Display Subsystem	EK-VTV01-TM
VSV01 IPB	EK-VSV01-IP

Table 1-3 Related Hardware Manuals and Documents (Cont)

Title	Part Number
Conrac Model 5500 Color Monitor Maintenance Manual	No DEC part number assigned
KW11-P Programmable Real-Time Clock Manual	EK-KW11P-MM
KW11-P PM Procedure	EK-KW11P-PM
VT52 DECscope Maintenance Manual	EK-0VT52-MM
VT52 DECscope IPB	EK-0VT52-IP
AR11 User's Guide	DEC-11-HARUG-B-D
Gamma-11 Operator's Guide	DEC-11-MGOGA-A-D
Corporate Site Preparation Guide	EK-CORP-SP
PDP11 Family Field Installation and Acceptance Procedure	EK-FS003-IN
NAD01 Manual (Northern Scientific)*	
NAD01 Manual (ORTEC)*	
NIMBIN Manual (TENNELEC)*	
NIMBIN Manual (ORTEC)*	

* Dependent on type of equipment in the system

CHAPTER 2

CHAPTER 2
SITE PREPARATION AND PLANNING

The primary reference document for site preparation and planning information is the Corporate Site Preparation Guide, part number EK-CORP-SP. The purpose of this chapter is to supplement that document with specific Gamma-11 site preparation and planning considerations.

2.1 FURNITURE REQUIREMENTS

Chairs, tables, and storage cabinets are not included as part of the Gamma-11 System hardware supplied by Digital Equipment Corporation. The customer is responsible for providing these items for the proper and convenient use of the system.

An office chair, preferably on casters, is required at the LA36 DECwriter II computer console terminal. When a foreground/background system is ordered, an additional chair and a table are required for the VT52 DECscope terminal included with F/B configurations. The table must be capable of supporting the VT52 weight, which is approximately 20 kg (44 lb).

A table is required to support the VRV01 Color Video Monitor, which weighs approximately 23 kg (50 lb). The VRV01 is used to analyze data and needs to be viewed by the operator sitting at the LA36; the table surface should be 36 inches above the floor. The top of the processor cabinet can be used for this purpose if a table is not available.

Storage space is required for storage of disks, system documentation and for the CU5-B Camera Option. The camera storage requirement is 2 ft × 2 ft and should be reasonably dust-free.

2.2 CAMERA CABLE LENGTH

25-foot cables are supplied by Digital Equipment Corporation to connect the Gamma Cameras to the Gamma-11 System. If these cables are to be routed through any walls or ceilings, the customer must have the holes drilled and any conduit installed before the Gamma-11 System is installed. When the system arrives on site, the cables should be immediately laid out, while the equipment is being checked, so that connections can be made as soon as the Field Service engineer is ready.

If the standard 25-foot cables aren't long enough, longer cables will have to be ordered. However, because Digital Equipment Corporation has no control over the Gamma Camera output, any cables longer than 25 feet are to be installed at the customer's risk. For example, if nonstandard cables cause camera output signal degradation, the problem will have to be solved by the customer. Additional electronics may need to be purchased, by the customer, to restore camera signals degraded by excessive cable lengths.

CHAPTER 3

CHAPTER 3
INSTALLATION

This chapter contains installation information related to the Gamma-11 System, in general, and the NC11-A interface in detail. The information presented includes system cabling, gamma signal levels, and system checkout. The purpose of this chapter is to supplement existing installation information contained in documents listed in Chapter 1, Table 1-3.

3.1 GENERAL INSTALLATION INFORMATION

Step-by-step procedures for unpacking, inspecting and checkout for the PDP11/34 Computer System, and other peripheral equipments relating to the Gamma-11 System are contained in referenced documents listed in Table 1-3. In addition, grounding information is presented in Digital's Site Preparation Guide, part number EK-CORP-SP.

3.2 CABLE INSTALLATION

The following paragraphs present the cabling information necessary for interconnecting all subassemblies of the Gamma-11 System. See Figures 3-1 and 3-2. The Gamma-11 System layout is illustrated in Figure 3-3. Unibus assignments are listed in Table 3-1.

3.2.1 VRV01 Color Video Graphics Display

The VRV01 Color Video Graphics Display is connected to the A011 Analog Output Module of the VTV01 Color Video Controller using scope cable part number 70-11961-25. Refer to drawing number D-IC-VSV01-0-1 in the VSV01 Field Maintenance Print Set (order number MP00063). Installation is made by performing the following.

1. Connect the cable to the SYNC (S), RED (R), GREEN (G), and BLUE (B) BNCs as shown. (Figure 3-1)

2. A short coaxial cable, part number 70-09991-01 should be connected between the TEST CH B and the remaining GREEN jack.

3. The extra RED and BLUE connectors are to be terminated with 75-ohm terminators secured next to the jacks on chains.

4. The extra SYNC connector is to be terminated with a 125-ohm terminator, part number 53-08798-3.

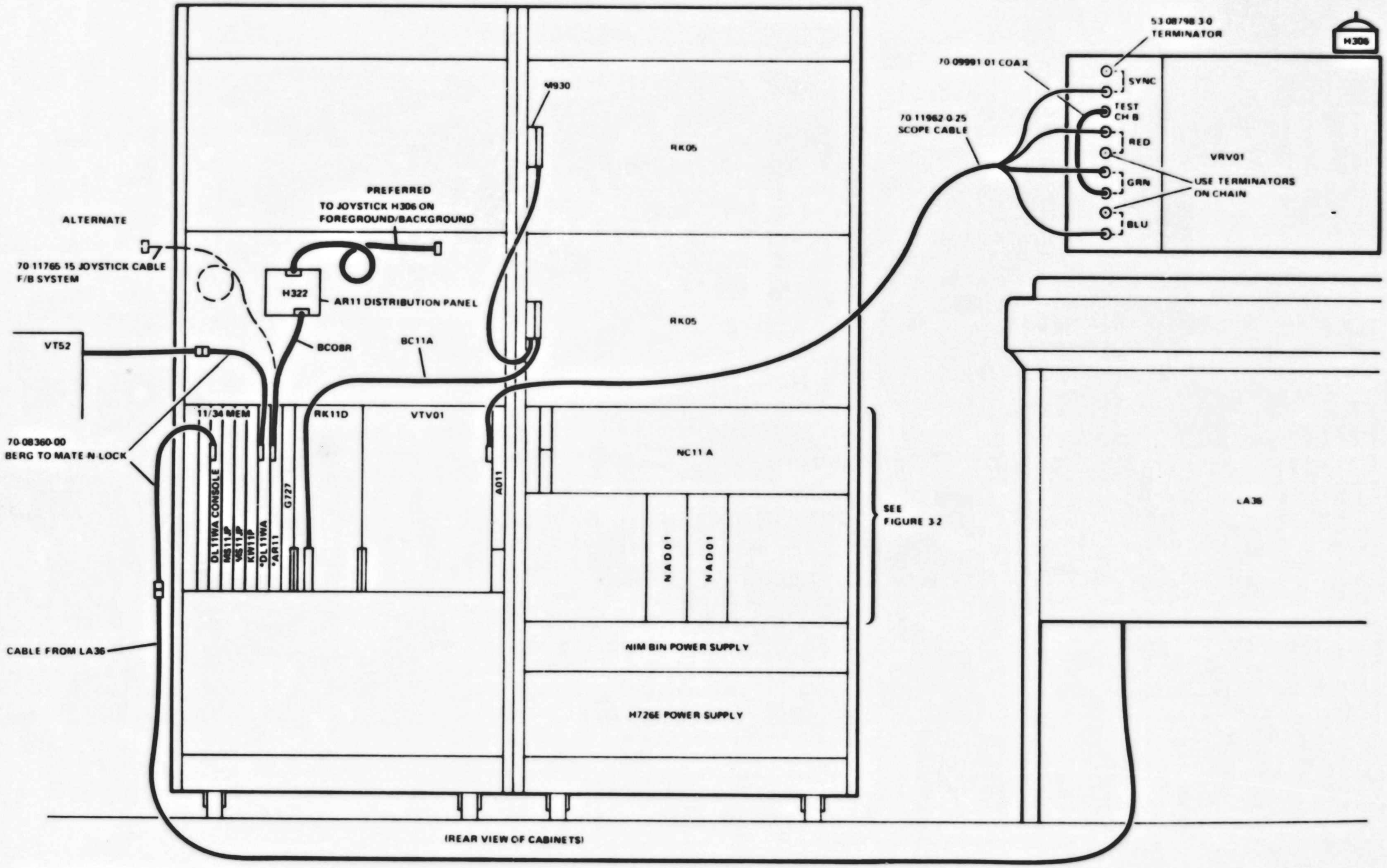
The 40-pin Berg connectors on the VTV01, M7067 and M7068 modules are provided for factory-test purposes and are not used in the Gamma-11.

NOTE

All open slots on the VTV01 backplane are to remain open. These slots are not SPC slots and do not require installation of BG cards.

Table 3-1 Unibus Assignment

Device	Address	Vector	Br Level
DL11-W	777560	60	4
Console Terminal	66	64	4
DL11 Terminal	776500	300	4
	06	304	4
Line Clock (p/o DL11-W)	777546	100	6
KW11P	772540	104	6
	44		
RK11D	777400	220	5
	16		
AR11 A/D	770400	340	6
AR11 Clock		344	6
AR11 Display	16	350	4
NC11-A Interface	764000	270	7
	14	274	7
M9301 Boot	773000	-	-
	777		
	765000		
	777		
VTV01	772600	360	4
	56		
RK611	777440	210	5
	76		


ALTERNATE
70 11765 15 JOYSTICK CABLE
F/B SYSTEM
PREFERRED
TO JOYSTICK H306 ON
FOREGROUND/BACKGROUND
H322
AR11 DISTRIBUTION PANEL
VT52
BC08R
BC11A
M930
RK05
RK05
70-08360-00
BERG TO MATE-N-LOCK
11/34 MEM
DL11WA CONSOLE
MS11JP
MS11JP
KW11P
*DL11WA
*AR11
G727
RK11D
VTV01
A011
NC11 A
NAD01
NAD01
SEE
FIGURE 3-2
NIM BIN POWER SUPPLY
H726E POWER SUPPLY
CABLE FROM LA36
(REAR VIEW OF CABINETS)
53 08798 3 0
TERMINATOR
70 09991 01 COAX
70 11962 0 25
SCOPE CABLE
SYNC
TEST
CH B
RED
GRN
BLU
USE TERMINATORS
ON CHAIN
VRV01
H306
LA36
MR 0975

*ON GM11 FOREGROUND/BACKGROUND ONLY
G727 ON GM11 SINGLE JOB

Figure 3-1 Gamma-11 Interconnection Diagram

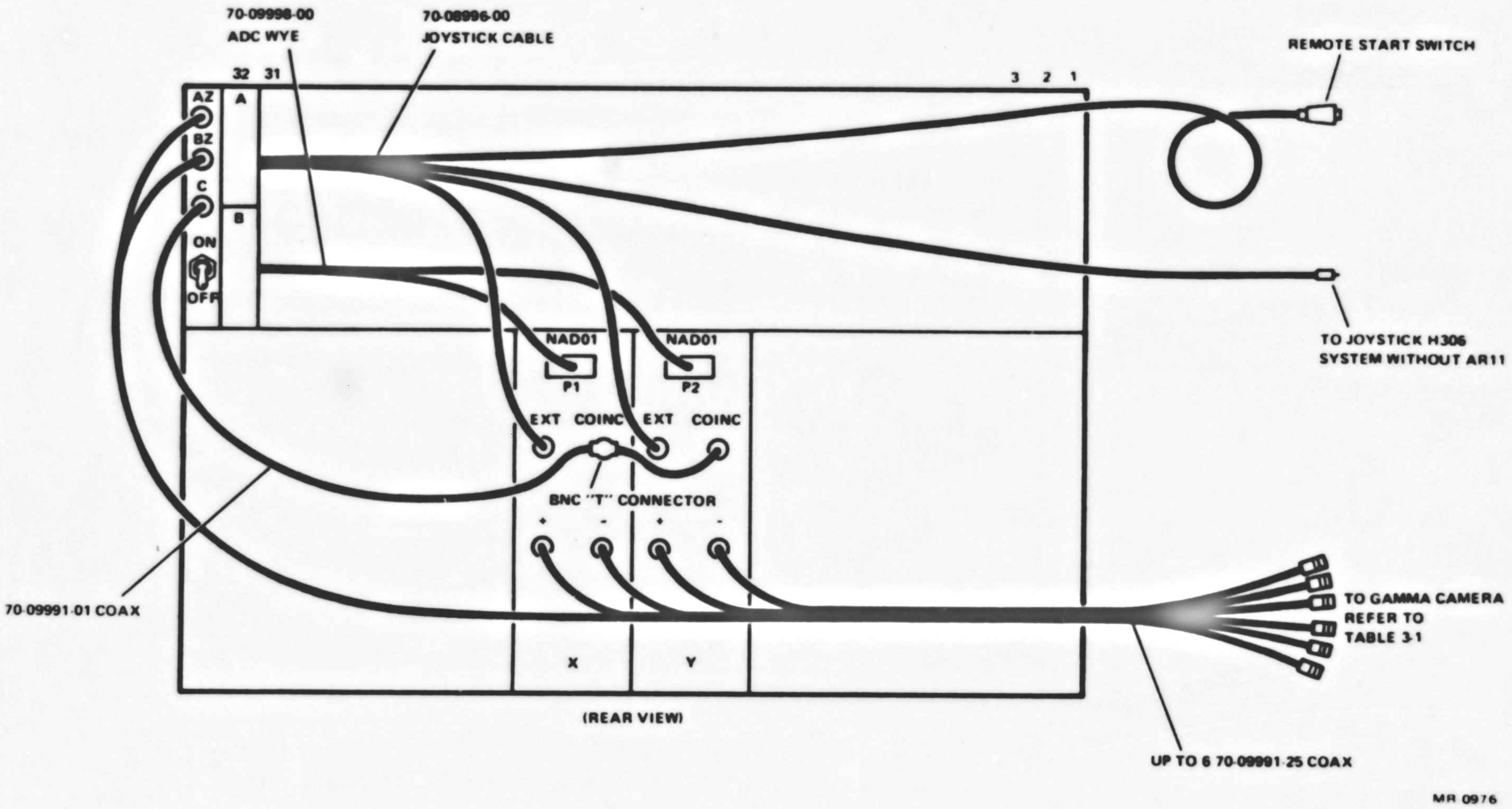

70-09998-00
ADC WYE
70-08996-00
JOYSTICK CABLE
REMOTE START SWITCH
32 31
3 2 1
AZ
BZ
C
A
B
ON
OFF
TO JOYSTICK H306
SYSTEM WITHOUT AR11
NAD01
P1
NAD01
P2
EXT COINC EXT COINC
BNC "T" CONNECTOR
+ - + -
70-09991-01 COAX
TO GAMMA CAMERA
REFER TO
TABLE 3-1
X
Y
(REAR VIEW)
UP TO 6 70-09991-25 COAX
MR 0976

Figure 3-2 Interconnection Diagram for NC11A Interface

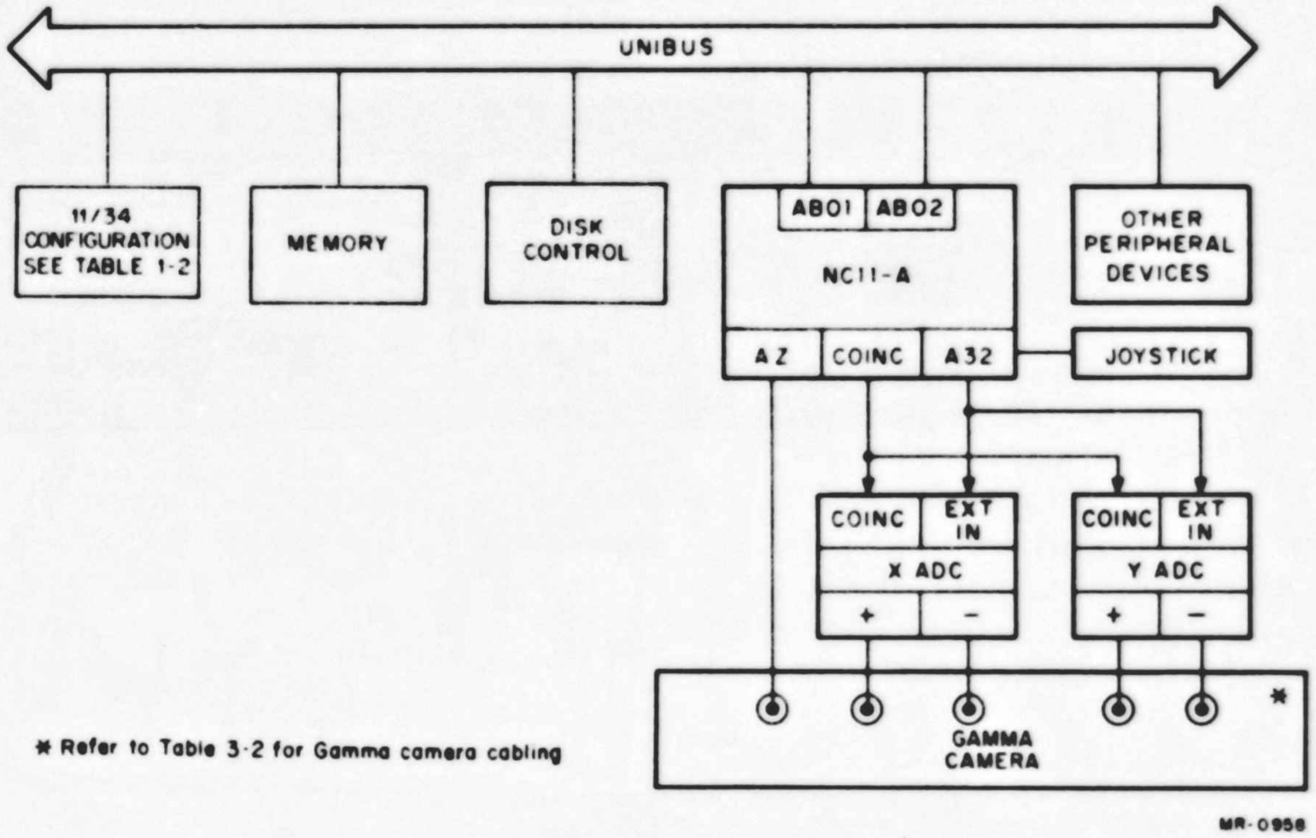

UNIBUS
11/34
CONFIGURATION
SEE TABLE 1-2
MEMORY
DISK
CONTROL
AB01
AB02
NC11-A
AZ
COINC
A32
OTHER
PERIPHERAL
DEVICES
JOYSTICK
COINC
EXT
IN
X ADC
+
−
COINC
EXT
IN
Y ADC
+
−
*
GAMMA
CAMERA
* Refer to Table 3-2 for Gamma camera cabling
MR-0958

Figure 3-3 Gamma System Layout

3.2.2 LA36 DECwriter II Keyboard Printer Terminal

The LA36 DECwriter II Keyboard Printer Terminal is connected to the DL11W Console board located in the BA11-K Mounting Box. A BC05F-15 20 mA cable is inserted into the 8-pin Mate-N-Lok connector attached to the DL11W Console board.

NOTE
The Unibus device address of the DL11W is 777560.

3.2.3 VT52 DECscope Display Terminal

The VT52 DECscope Display Terminal is connected to the DL11W Serial Line Asynchronous interface board using cable assembly 70-08360-0. This provides the Gamma-11 with a Foreground/Background capability. The address is 776500 with a vector of 300.

3.2.4 RK05 and RK06 Single Access Disk Drive

The two RK05 Single Accesss Disk Drives are connected to the RK11D Disk Drive Controller module using a BC11A cable.

When the RK06 single access disk drives are used, connections are made as described in RK611/RK06 Disk Subsystem Installation Manual (EK-RK611-IM).

3.2.5 H306 Joystick

The connection of the H306 Joystick varies depending on which configuration is used. Cable number 70-11765-15 is used to connect the Joystick to the H322 Distribution Panel attached to the AR11 Analog Real-time subsystem module for Foreground/Background configuration. Cable number 70-08996-0-0 is used to connect the Joystick to slot A32 on the NC11-A Interface for Single Job configuration. (Refer to Figure 3-2.)

3.2.6 NC11-A Interface

The NC11-A Interface receives inputs from the two NAD01 A/D connectors, the Gamma Camera and the H306 Joystick (for Single Job configuration) (see Figure 3-2). Slots AB01 and AB02 on the NC11-A Interface provides interfacing to the Unibus.

Perform the following procedure in installing cables to the NC11-A interface (refer to Figure 3-2).

1. Connect the ADC wye cable, part number 70-09998-0-0, from NC11-A slot B32 to both P1 and P2 on the NAD01 A/D Converter modules.

2. Connect the paddleboard of the joystick cable, part number 70-08996-0-0, into NC11-A slot A32.

3. Connect the two BNC coaxial cable connectors (part of joystick cable) to the EXT INPUT connectors on the rear panels of the NAD01 A/D Converter modules.

4. Run the thin coax with the remote start switch from A32 (p/o joystick cable) to the Gamma Camera console.

5. When the Gamma-11 System does not include the AR11, connect the heavy gray cable of the joystick cable assembly to the H306 joystick.

6. When the Gamma-11 System includes the AR11, coil up the heavy gray cable in the bottom of the cabinet. Use the Joystick cable, part number 70-11765 to connect the H306 to the AR11 (see Figure 3-1).

   When an H322 Distribution panel is used, the H306 Joystick is cabled to the H322 Distribution panel using Part #70-11765-15 cable (see 70-11765 wire table for connections). Connect cable BC08R from the H322 panel to the AK11.

7. Connect a 1-foot coaxial cable, part number 70-09991-01 from the COINC BNC connector on the NC11-A end panel to the BNC TEE COINC connector, part number 12-09746 on the X NAD01 ADC. The X NAD01 is the A/D converter that is closer to the power switch on the NIMBIN power supply.

8. Use a second 1-foot coaxial cable to connect from the BNC TEE connector on the X NAD01 to the COINC jack on the Y NAD01.

3.2.7 NAD01 A/D Converter

The NAD01 A/D converters used in the Gamma-11 System are manufactured by two different vendors: Northern Scientific Inc., and Ortec Inc. (see Figures 3-4 and 3-5). The Northern Scientific Inc. NAD01 Converter can be distinguished by the existence of a "% DEAD TIME" Meter located in the front panel and the six BNC jacks located on the rear.

Cable connections required for connecting the NAD01 converters to the NC11-A Interface are described in Paragraph 3.2.6. Add shorting plugs to Input 2+ and Input 2– on NAD01 A/D converters manufactured by Northern Scientific Inc.

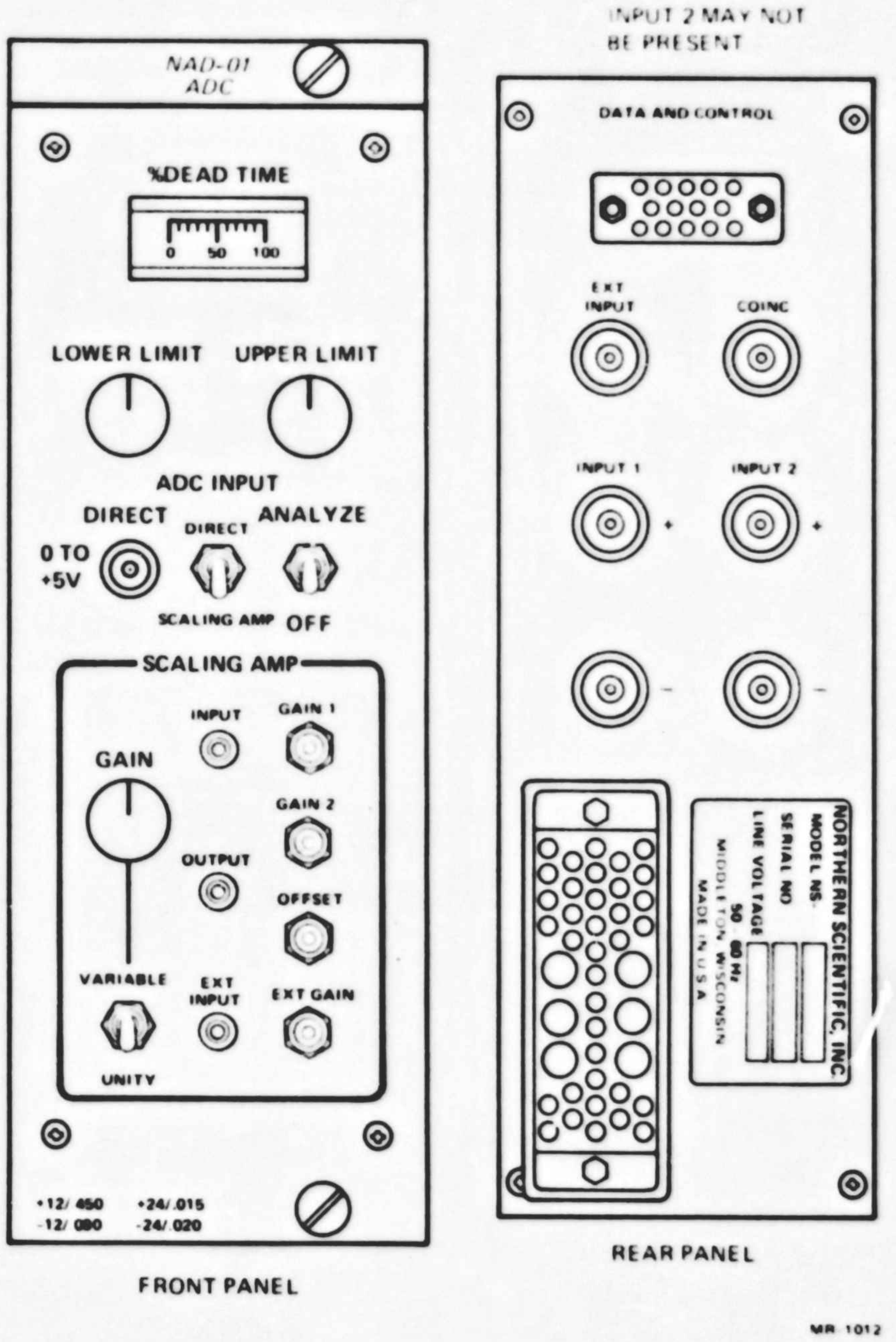

INPUT 2 MAY NOT BE PRESENT
NAD-01 ADC
%DEAD TIME
0 50 100
LOWER LIMIT
UPPER LIMIT
ADC INPUT
DIRECT
DIRECT
ANALYZE
0 TO +5V
SCALING AMP
OFF
SCALING AMP
INPUT
GAIN 1
GAIN
GAIN 2
OUTPUT
OFFSET
VARIABLE
EXT INPUT
EXT GAIN
UNITY
+12/ 450
-12/ 080
+24/.015
-24/.020
FRONT PANEL
DATA AND CONTROL
EXT INPUT
COINC
INPUT 1
INPUT 2
+
+
–
–
NORTHERN SCIENTIFIC, INC
MODEL NS-
SERIAL NO
LINE VOLTAGE
50 - 60 Hz
MIDDLETON, WISCONSIN
MADE IN U.S.A.
REAR PANEL
MR 1012

Figure 3-4 NAD01 ADC (Northern Scientific Inc.)

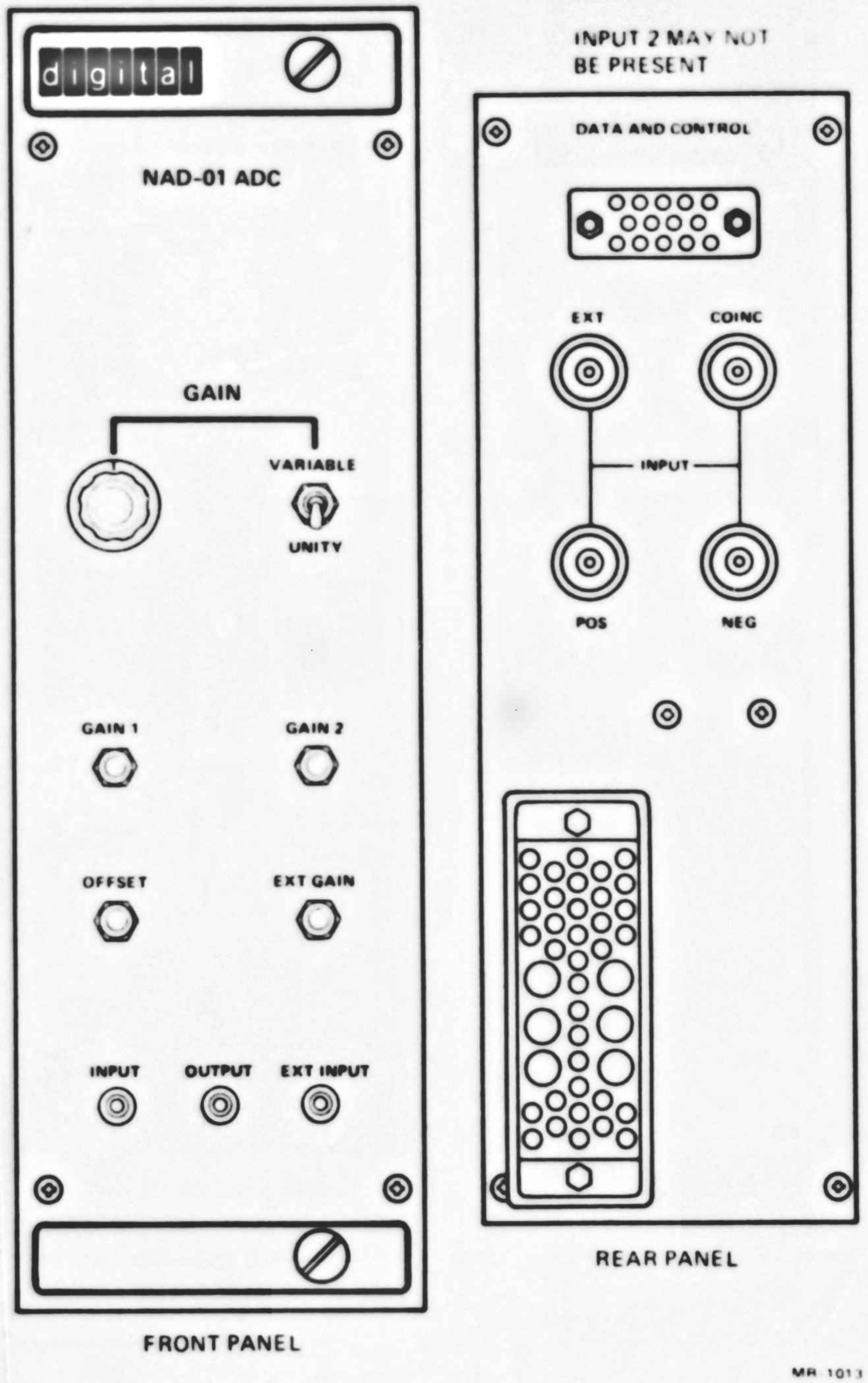


Figure 3-5 NAD01 ADC (Ortec Inc.)

3.2.8 Gamma Camera

All connections from the Gamma Camera to the NC11-A Interface and two NAD01 converters are made using up to six coaxial cables (part number 70-09991-25). The cable connections are listed in Table 3-2. The connections vary depending on whether the camera signals at the camera console are differential or single ended. More detailed information on these signals is presented in Paragraph 3.3. Refer to Gamma System layout Figure 3-3 for interconnection of camera to the Gamma-11 System.

NOTE

It is recommended to verify the output signals from the camera as presented in Paragraph 3.3.

Table 3-2 Gamma Camera Cabling

Camera	NAD01X		NAD01Y		NC11A	
	1+	1-	1+	1-	ZA	ZB
Searle Pho Gamma 5 single ended	X⁺ Input	Shorting Plug	Y⁺ Input	Shorting Plug	Z⁺ Input	
Ohio Nuclear I/O Universal Interface Bd single ended	Shorting Plug	X	Shorting Plug	Y	Z	
Picker single ended DYNA 4	X Input +	Shorting Plug	Y Input +	Shorting Plug	Z Input	
GE single ended	Shorting Plug	X	Shorting Plug	Y	Z	
Raytheon	Shorting Plug	X	Shorting Plug	Y	Z	
Elcint	X	Shorting Plug	Y	Shorting Plug	Z	

*ZB for Dual Isotope, otherwise use shorting plugs.

**Required to provide position Z pulses and increase the X and Y pulse width.

3.3 GAMMA CAMERA SIGNAL LEVELS

The Gamma Camera signal requirements are presented in the following paragraphs. Presented are acceptable Gamma signal characteristics for the X, Y and Z pulses.

Since all cameras used with the Gamma-11 System are vendor items, the customer has the responsibility to ensure that proper camera signals are available.

The Gamma Camera provides two sets of signals to the NC11-A and NAD01 A/D converters. The first set consists of Analog X and Y signals, the second is an unblank or "Z" pulse which indicates when the analog X and Y signals are valid.

3.3.1 Analog X and Y Pulses

The amplitude of the X and Y pulses represent the positioning of the Gamma rays on the camera. A larger amplitude X pulse will result in the Gamma rays appearing further to the right on the camera; a larger amplitude Y pulse results in rays appearing higher on the camera.

The NAD01 converters have the capability to amplify a variety of input signals to provide the proper amplitude signal. However, due to the limited range of these amplifiers, the signals must meet the specification depicted in Figure 3-6.

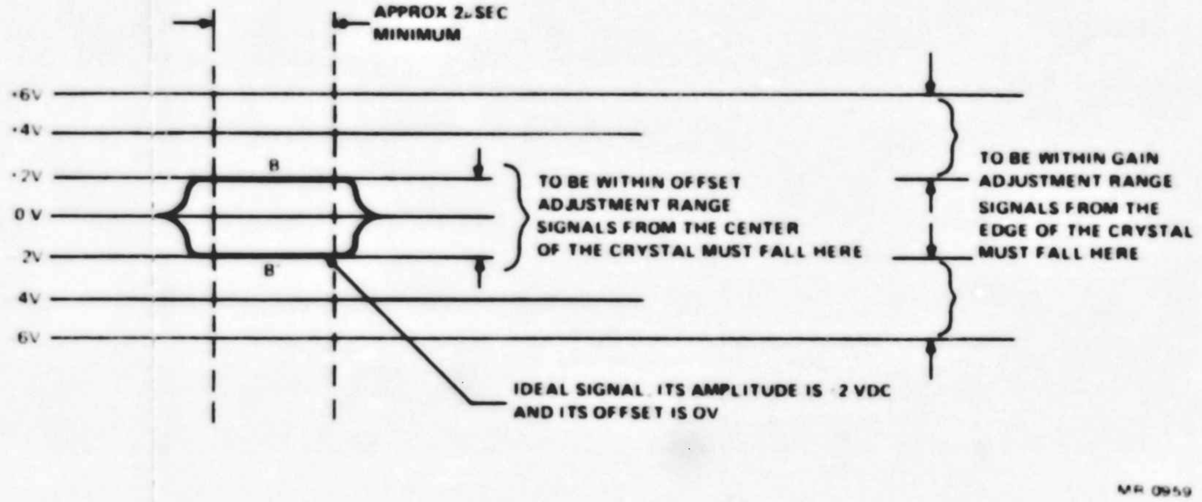

APPROX 2µSEC MINIMUM
+6V
+4V
+2V
0 V
2V
4V
6V
B
B'
TO BE WITHIN OFFSET ADJUSTMENT RANGE SIGNALS FROM THE CENTER OF THE CRYSTAL MUST FALL HERE
TO BE WITHIN GAIN ADJUSTMENT RANGE SIGNALS FROM THE EDGE OF THE CRYSTAL MUST FALL HERE
IDEAL SIGNAL. ITS AMPLITUDE IS 2 VDC AND ITS OFFSET IS OV
MR 0959

Figure 3-6 X and Y Signal Characteristics

3.3.2 Unblank Z Pulse

The Z pulse enters the NC11-A through a Schmitt trigger (M501). For normal operation, this pulse is positive going up to at least 3 volts (for 250 ns) and descends to within 0.6 V of ground. This pulse may increase to +20 volts and decrease to -20 volts. However, the output is true beyond +2 volts and remains true until the trailing edge drops to 1 volt (see Figure 3-7).

3.3.3 Acceptable Signal Levels

Illustrated in Figures 3-6 and 3-7 are acceptable camera signal characteristics for the X, Y and Z pulses.

Signal B represents the highest amplitude output signal from the Gamma Camera. (Refer to Figure 3-6.) Signal B is the output of the Gamma Camera console when the information is at one edge of the detector crystal and B' is the signal when the information is at the opposite edge. A pulse height of zero volts would denote information from the center of the detector. The B signal dc levels are 6 volts maximum and 2 volts minimum.

The Gamma Camera Z input signal requirements are illustrated in Figure 3-7. Input loading is 2.7 K ohms to +5 volts. The Z signal source must be capable of sinking 1.8 mA to ground. Input signal must be limited to ±20 volts.

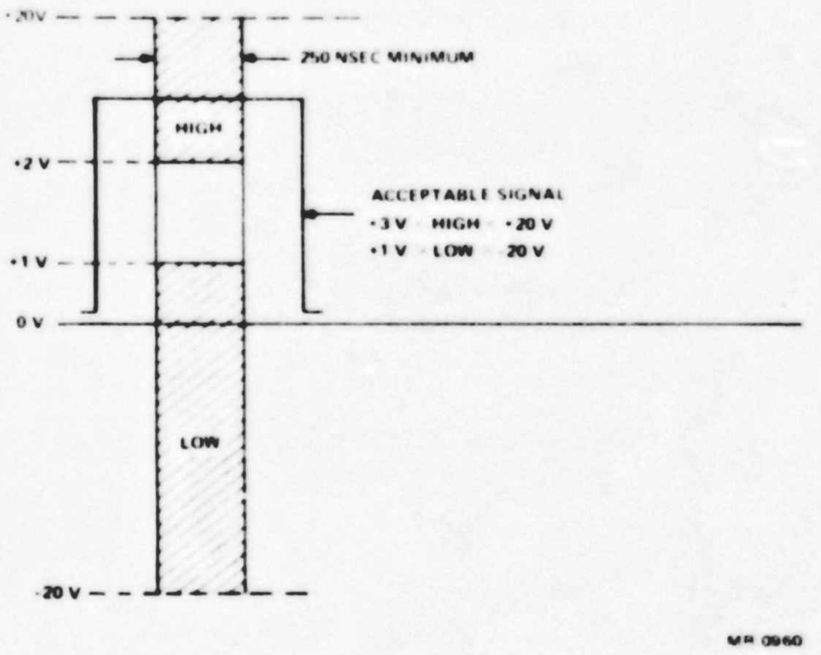

+20V
250 NSEC MINIMUM
HIGH
+2 V
ACCEPTABLE SIGNAL
+3 V HIGH +20 V
+1 V LOW 20 V
+1 V
0 V
LOW
-20 V
MR 0960

Figure 3-7 Z Signal Characteristics

3.3.4 Gamma Camera Manufacturers

The Gamma Cameras used in the Gamma-11 System are vendor items. Five of the manufacturers currently supplying these cameras are listed in Table 3-3. Signal connections, adjustments and relative timing for each camera are present in this section. Any internal connections or adjustments necessary to the camera to obtain proper signals must be made by the camera representative.

3.3.4.1 Raytheon Cameras

1. Signal Connections - The camera X, Y and Z BNC connectors are located behind the lower cover on the back of the camera console cabinet. The connectors are in a vertical row at the left-most end of the backplane. Connect the X, Y and ZA cables from the NC11-A to the BNC connectors marked X, Y and Z, respectively.

2. Signal Adjustments - Both models of the Raytheon Nuclear camera must have an Interlog Interface Board plugged into the right-most slot in the module cage. There are two orientation switches on the board that can be used to invert the image acquired by the NC11-A. Any necessary adjustments to the camera electronics should be made by the camera vendor representative.

   The signal names, amplitude, and relative timing for the Raytheon cameras are illustrated in Figure 3-8.

Table 3-3 Camera Manufacturers

Manufacturer	Model No.	
Raytheon	Camera 91 (XL91) Cameray II	
Searle	LEM Pho Gamma 5 LFOV	Similar Electronics
	Pho Gamma 4 Pho Gamma HP (6506)	Similar Electronics
Picker	Dyna Camera 4 Dyna MO Portable	Similar Electronics
	Dyna camera 2C, 3C	
Ohio Nuclear		
Elcint	CE 1719 Dymax SPR -11-Q -11-LF	

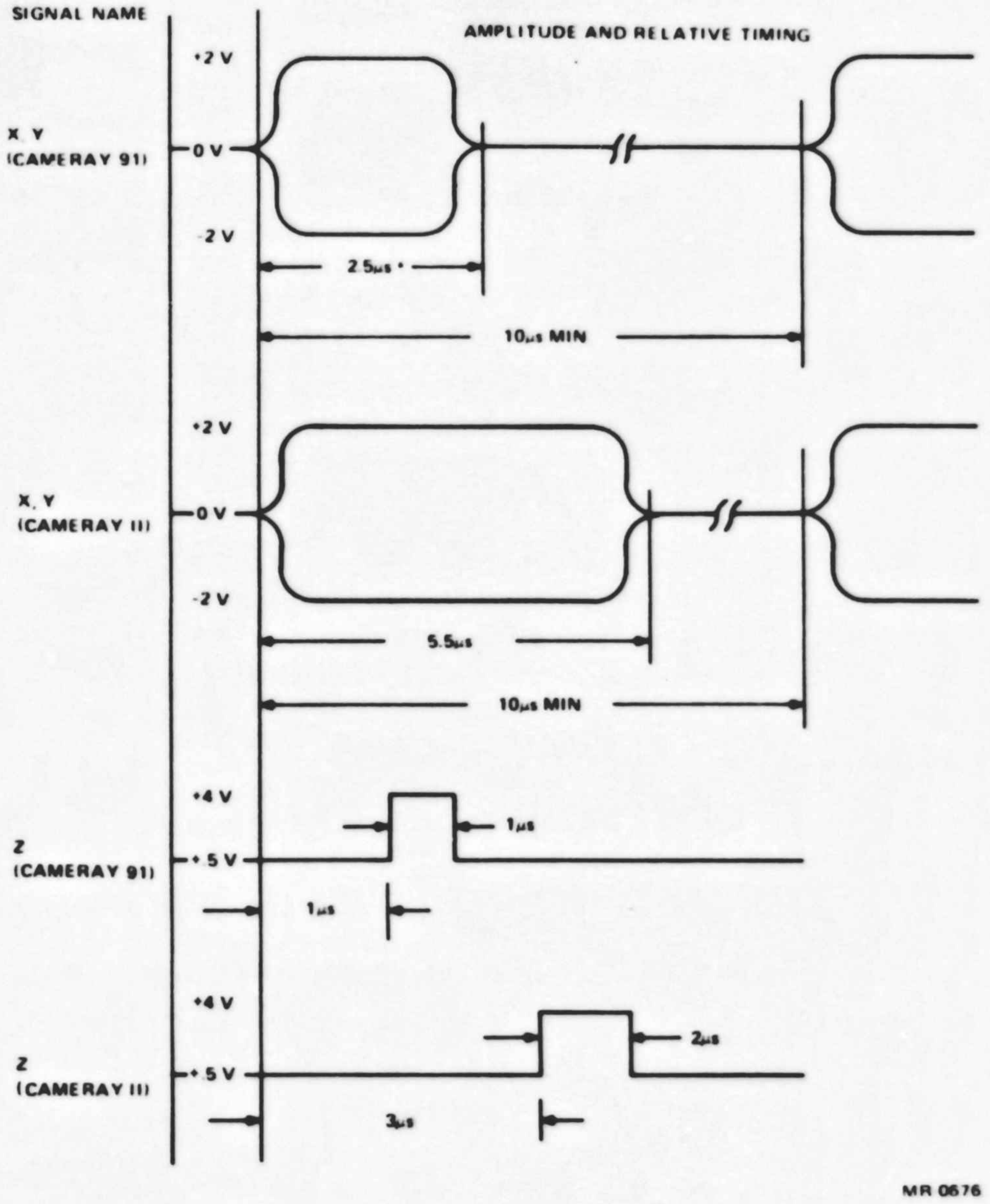

SIGNAL NAME
AMPLITUDE AND RELATIVE TIMING
X, Y (CAMERAY 91)
+2 V
0 V
-2 V
2.5μs
10μs MIN
X, Y (CAMERAY II)
+2 V
0 V
-2 V
5.5μs
10μs MIN
Z (CAMERAY 91)
+4 V
+.5 V
1μs
1μs
Z (CAMERAY II)
+4 V
+.5 V
2μs
3μs
MR 0676

Figure 3-8 Raytheon Nuclear Camera Signals

3.3.4.2 Searle Cameras

1. Signal Connections - Signal connections to all five Searle cameras are made on the rear of the Persistence Scope (part of the camera) which is located on top of the console cabinet. The scope can rotate 360 degrees, and in some cameras it can be raised, so allow enough slack in the cables to provide this movement. The NC11-A and camera cables are connected to the scope with BNC-TEE connectors. The connectors are provided with the NC11-A.

   a. Install the BNC-TEE connectors on the X+ input, Y+ input, and Z+ input connectors on the scope.

   b. Connect the NC11-A X, Y and ZA and camera X, Y and Z cables to the X, Y and Z +BNC-TEE connectors on the Persistence Scope.

2. Signal Adjustments - Any necessary adjustments to the camera electronics should be made by the camera vendor representative. The signal names, amplitude and relative timing for the Searle cameras are illustrated in Figure 3-9.

3.3.4.3 Picker Cameras

1. Signal Connections - The following presents signal connections for three of the Picker cameras.

   DYNA CAMERA 4 - BNC connectors for X out and Y out and a "D" connector for J109 (input/output) are visible on the back of the console cabinet. The Picker interface box connects to J109 and provides the ZA and ZB signals to two BNC connectors on the box.

   NOTE
   The interface box is necessary to amplify the signals to an acceptable level.

   Connect the NC11-A X and Y cables to the X out and Y out BNC connectors on the console cabinet and the ZA and ZB cables to the ZA and ZB connectors on the interface box.

   DYNA MO - BNC connectors are provided behind the rear doors. Connect the NC11-A X and Y cables to the X out and Y out connector and the ZA and ZB cables to the ZA and ZB connectors on the camera.

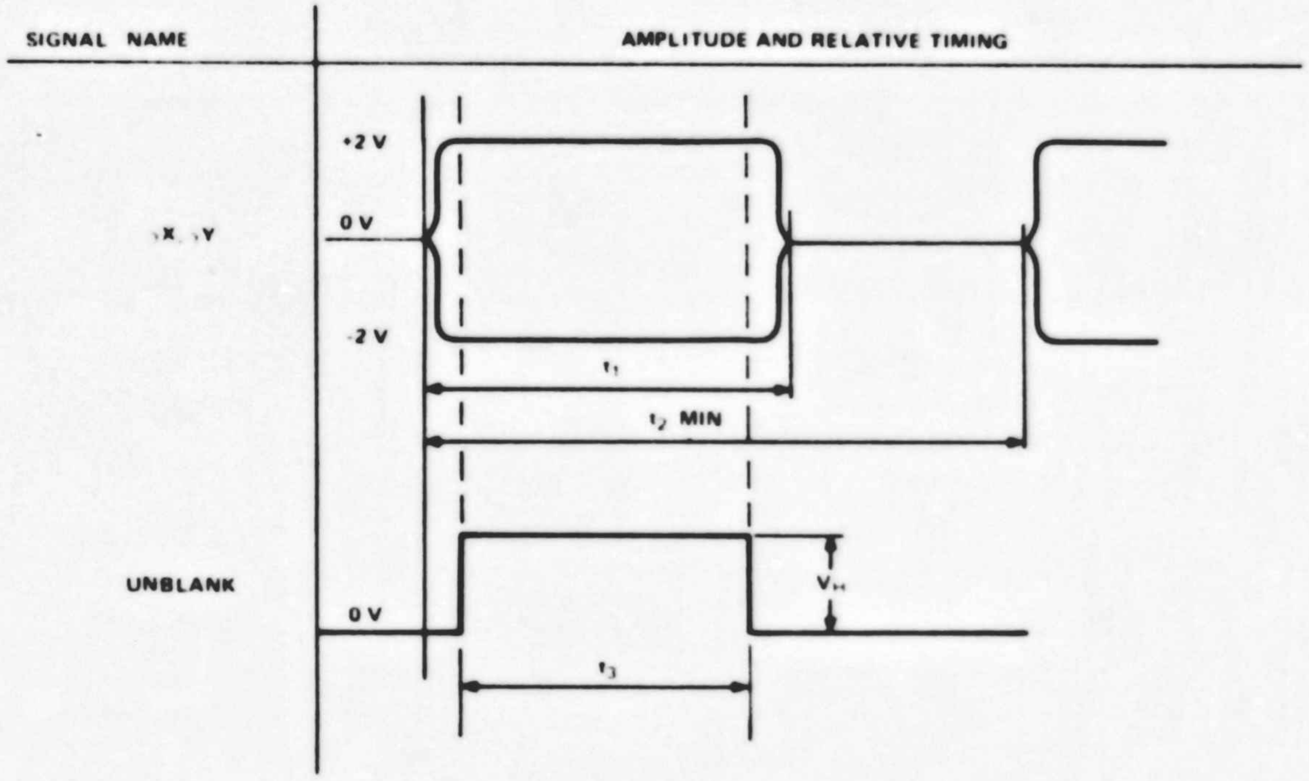
   DYNA CAMERA 2C, 3C - A Tektronix 602 display scope is mounted at the left side of the camera console cabinet. Loosen the two twist lock screws holding the side panel and remove the panel to gain access to the BNC connectors on the back of the scope.

   Connect the X and Y cables from the NC11-A to the X and Y BNC connectors on the display scope.

   With an external oscilloscope on the Z output of the camera, turn the intensity knob on the camera console until a Z pulse with a minimum amplitude of +3 V is attained.

   Disconnect the external scope and connect the NC11-A ZA cable to the Z connector on the display scope.

   Switch the camera to ANALOG to attain acceptable X and Y signals.



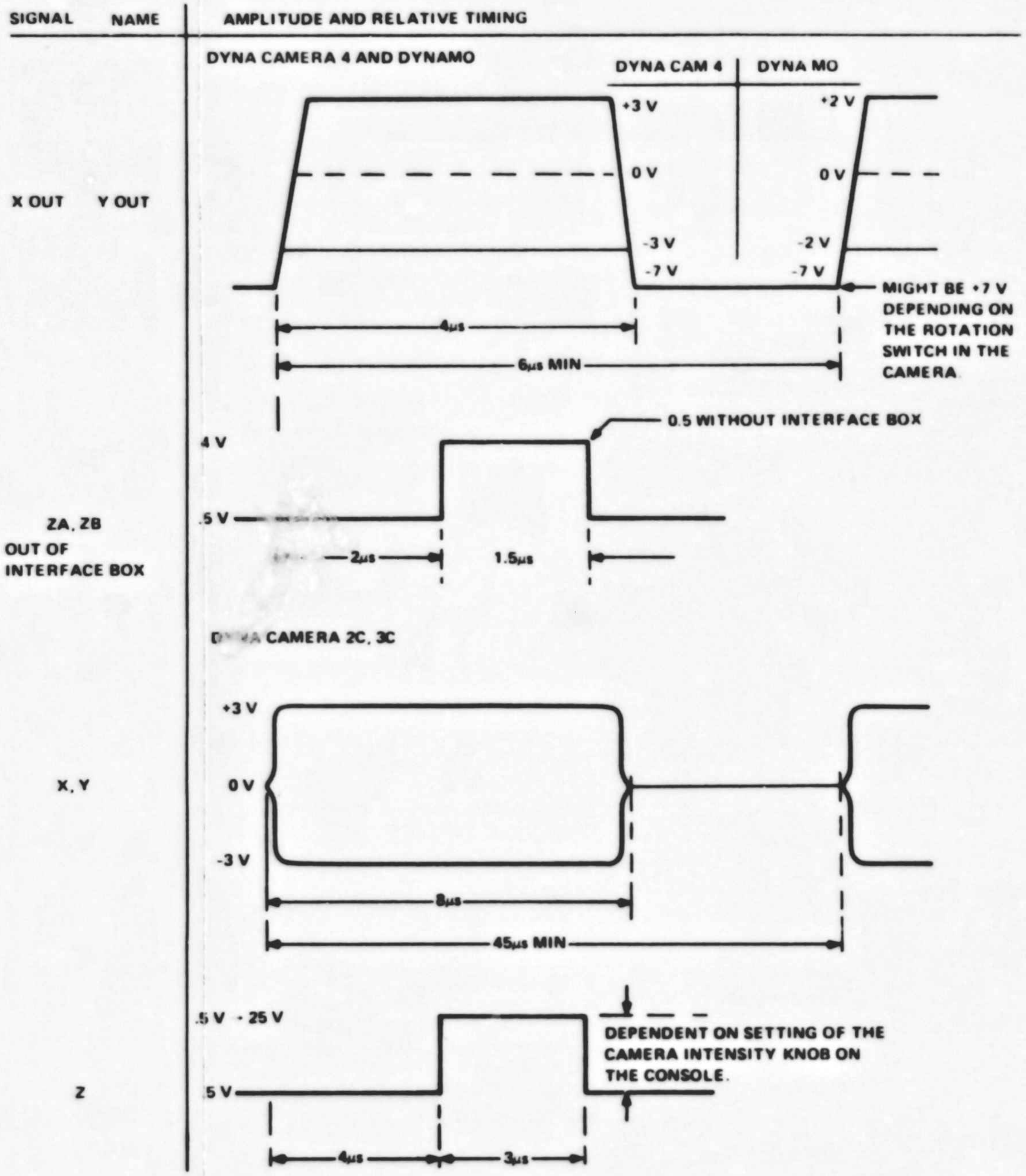
LEM, LFOV AND PHO GAMMA 5		PHO GAMMA 4 AND HP	
t_1	2μs - 13μs	t_1	2μs - 13μs
t_2	4.5μs MINIMUM	t_2	10μs MINIMUM
t_3	2μs - 10μs (MUST FALL WITHIN TIME ENVELOPE t_1 AND MUST COINCIDE WITH THE FLAT PORTION OF X, Y PULSE)	t_3	2μs - 10μs (MUST FALL WITHIN TIME ENVELOPE t_1 AND MUST COINCIDE WITH THE FLAT PORTION OF X, Y PULSE)

MR-0653

Figure 3-9 Searle Nuclear Camera Signals

2. Signal Adjustments - Any necessary adjustments to the camera electronics should be made by the camera vendor representatives.

   The signal names, amplitude, and related timing for the Picker nuclear cameras are shown in Figure 3-10.


SIGNAL NAME
AMPLITUDE AND RELATIVE TIMING
DYNA CAMERA 4 AND DYNAMO
DYNA CAM 4
DYNA MO
+3 V
0 V
-3 V
-7 V
+2 V
0 V
-2 V
-7 V
X OUT Y OUT
MIGHT BE +7 V DEPENDING ON THE ROTATION SWITCH IN THE CAMERA.
4μs
6μs MIN
0.5 WITHOUT INTERFACE BOX
4 V
.5 V
ZA, ZB OUT OF INTERFACE BOX
2μs
1.5μs
DYNA CAMERA 2C, 3C
+3 V
0 V
-3 V
X, Y
8μs
45μs MIN
.5 V - 25 V
.5 V
Z
DEPENDENT ON SETTING OF THE CAMERA INTENSITY KNOB ON THE CONSOLE.
4μs
3μs

NOTE:
THE OUTPUT SIGNALS FROM THE DYNA CAMERA 4 ARE NOT ADEQUATE FOR THE NCV11. AN INTERFACE BOX IS NECESSARY TO BOOST THE SIGNALS.

MR 0660

Figure 3-10 Picker Nuclear Camera Signals

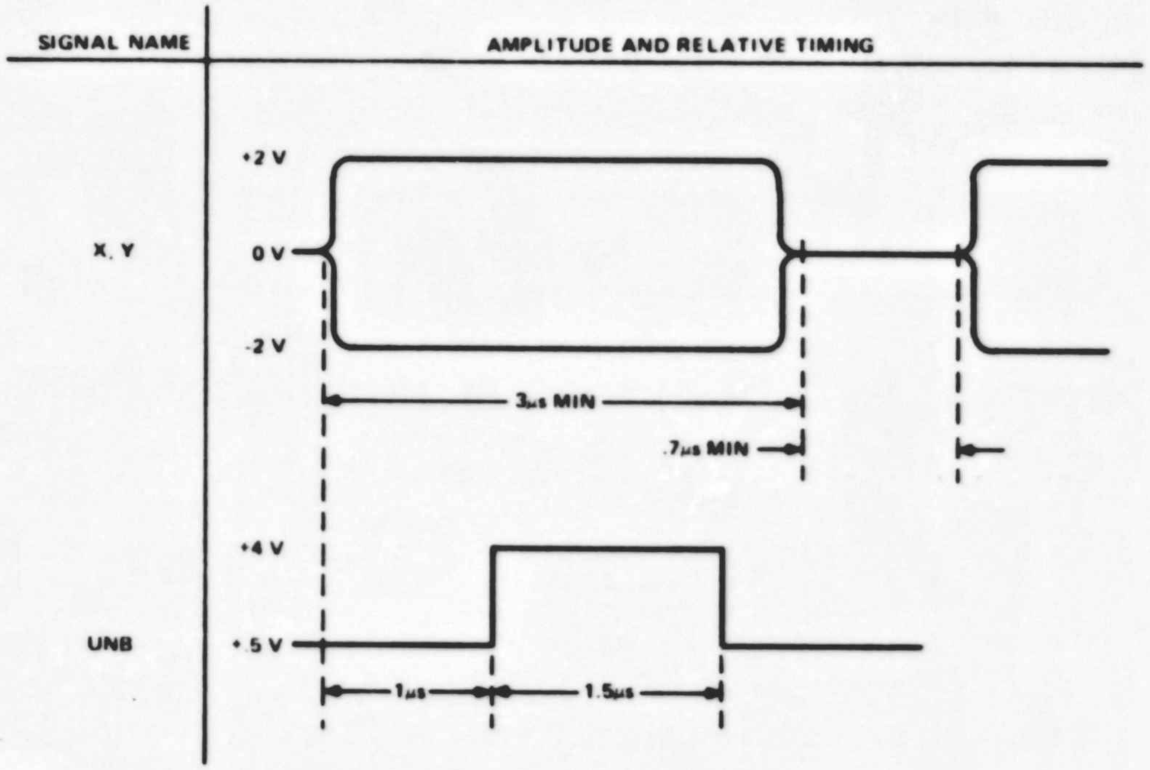
3.3.4.4 Ohio Nuclear Cameras

1. Signal Connections – Connect the X, Y, and ZA cables from the NC11-A to the 20-foot X, Y and UNB (Unblank) cables on the interface board.

CAUTION

The ZA Cable from the NC11-A MUST be connected to the UNB output connector from the camera. DO NOT connect it to the connector marked Z2 on the camera.

2. Signal Adjustments – Each Ohio Nuclear camera must have a Universal Interface board. There are adjustments that can be made on the Interface board to produce acceptable X, Y, and Unblank Z signals. These adjustments should be made by the camera vendor representative. See Figure 3-11 for the Ohio Nuclear Camera signals.


SIGNAL NAME
AMPLITUDE AND RELATIVE TIMING
+2 V
0 V
-2 V
X, Y
3μs MIN
.7μs MIN
+4 V
+.5 V
UNB
1μs
1.5μs

NOTE
A JUMPER ON THE INTERFACE BOARD DETERMINES THE POLARITY OF UNB. CHECK WITH THE VENDOR REPRESENTATIVE.

MR 0650

Figure 3-11 Ohio Nuclear Camera Signals

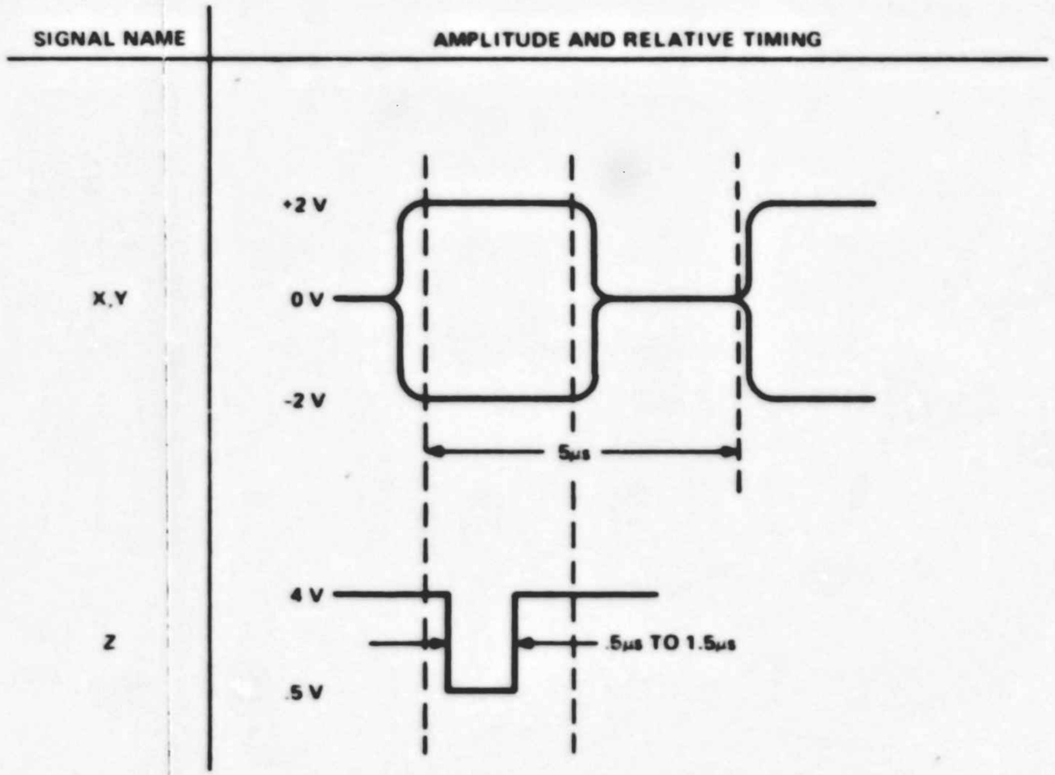
3.3.4.5 Elcint Cameras

1. Signal Connections - The X, Y, and Z output BNC connectors are located on the lower back of the camera console. On some of the more recent models, the back cover may have to be removed from the console cabinet to gain access to the BNC connectors.

   Connect the X, Y, and Z cables from the NC11-A to the X, Y, and ZA BNC connectors on the camera. If a dual-Isotope camera is being used, both the ZA and ZB cables from the NC11-A must be connected to the ZA and ZB BNC connectors on the camera.

   Signal Adjustments - The X and Y pulses provided by Elcint cameras may be too narrow for the NC11-A. Also, the Z pulse is inverted and may present a problem. If this is the case, enlist the aid of the Elcint Field Service Engineer in widening the X and Y pulses and providing a positive-going Z pulse.

   It is recommended that a camera vendor representative make all necessary adjustments to the camera electronics. Refer to Figure 3-12 for the Elcint Nuclear Camera Signals.



NOTE
X AND Y PULSES MAY BE TOO NARROW.
Z PULSE IS INVERTED AND MAY BE A
PROBLEM. CHECK WITH ELCINT FIELD
SERVICE.

Figure 3-12 Elcint Nuclear Camera Signals

3.3.5 Gate Synchronized Acquisition (GSA)

In GSA applications, it is necessary to synchronize the collection of data from the camera to an external gating signal derived from an ECG gating device. It is recommended that a Brattle Gate or similar triggering device be used to generate the gate signal. The signal must not be taken directly from the ECG monitor.

The gating signal should be a positive- or negative-going pulse with a duration between 1 ms and 400 ms. The high level should be at least 3 V with a logic low below 0.8 V. If this is a positive-going pulse, it should be applied to Channel 3 of the AR11. If a negative going pulse is used, it must be connected to the External Start input of the AR11. All connections should be made to the H322 Distribution Panel. If the External Start input or a Channel other than 3 is used, the software must be patched since the software is shipped expecting an input to Channel 3.

NOTE

Channels 0, 1, and 2 are reserved for the joystick and must not be used for the gating signal.

A shielded cable should be used to connect this gate to the Gamma-11 System. The shield should be connected to ground at the gate only. Refer to the AR11 Users Guide for detailed information concerning signal levels, grounding and pin connections.

3.4 INSTALLATION CHECKOUT

There are two program exercisers used in installation checkout: the System Exerciser (DEC-X-11) and the Gamma-11 Exerciser (MAINDEC-11-DZNCB). The following listing presents the software program available for checkout. Refer to Chapter 4 for additional information.

Test	**MAINDEC-11-**	**Run Time For Acceptance**
	KD11-E Processor	
Basic Instruction Test	DFKAA	15 min
Traps Test	DFKAB	15 min

NOTE

Use Rev B or later of DFKAB for the KD11-EA (M8265, M8266).

EIS Test	DFKAC	5 min
KT Logic	DFKTA	5 min
KT States	DFKTA	5 min
KT Keys	DFKTA	5 min
MTPI/MFPI	DFKTD	5 min
KT ABORT	DFKTF	5 min
KT Exerciser	DFKTG	15 min
MOS/CORE	DZKMA	2 passes

Power Fail	DZKAO	10 times
Parity Controller (M7850)	DCMFA	10 passes
LA36 DECWRITER (DL and KL)	DZLAZ	1 pass
KW11-P Programmer Clock		
Logic Test	DZKWB	15 min
NC11-A Gamma Camera Interface		
Logic Test	DZNCA	2 passes
Gamma-11 Exerciser	DZNCB	as required
RK11/RK05-RK05J 1.2M Disk		
Basic Logic 1	DZRKJ	2 passes
Basic Logic 2	DZRKK	2 passes per drive
Utility Package	DZRKI	
Formatter/Verifier		1 pass per drive
Compatibility		1 pass per drive
Power Fail		1 pass per drive
Dynamic Test	DZRKL	2 passes per drive
Performance Exerciser	DZRKH	4 hours per drive
RK611/RK06*		

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* Refer to Chapter 5 of RK611/RK06 Disk Subsystem Installation Manual.

CHAPTER 4

CHAPTER 4
TROUBLESHOOTING

This chapter presents methods for investigating causes of various failures and correcting faults that may occur at the system or subsystem levels. Information relating to adjustments are also included. All information presented in this chapter is intended to supplement existing troubleshooting procedures in the documents listed in Table 1-3.

4.1 SYSTEM TROUBLESHOOTING

The following information is included to aid in troubleshooting the Gamma-11 System. Each paragraph number corresponds to each step number presented in the flow chart illustrated in Figure 4-1.

4.1.1 Failure Detection

System failures can be categorized into three areas.

1. Hardware failure
2. Software problem
3. Operation error

It is recommended that the hardware be checked to determine which option, if any, is not operating properly.

4.1.2 Run DEC-X-11 Exerciser

The DEC-X-11 Exerciser is designed to check the Gamma-11 System and should define a faulty option. It is important when running the exerciser that the Maintenance Switch located on the side panel of the NC11-A, is placed in the up (ON) position.

NOTE

For intermittent problems, the DEC-X-11 Exerciser should run error free for at least twice as long as the average time between failures.

4.1.3 Run Gamma-11 Exerciser

Once the DEC-X-11 Exerciser has been run without error, load and run the Gamma-11 Exerciser (MAINDEC-11-DZNCB). This exerciser will check the operation of the NAD01 converters and connections to the Gamma Camera.

NOTE

The Gamma Camera should be running at about 30,000 counts per second.

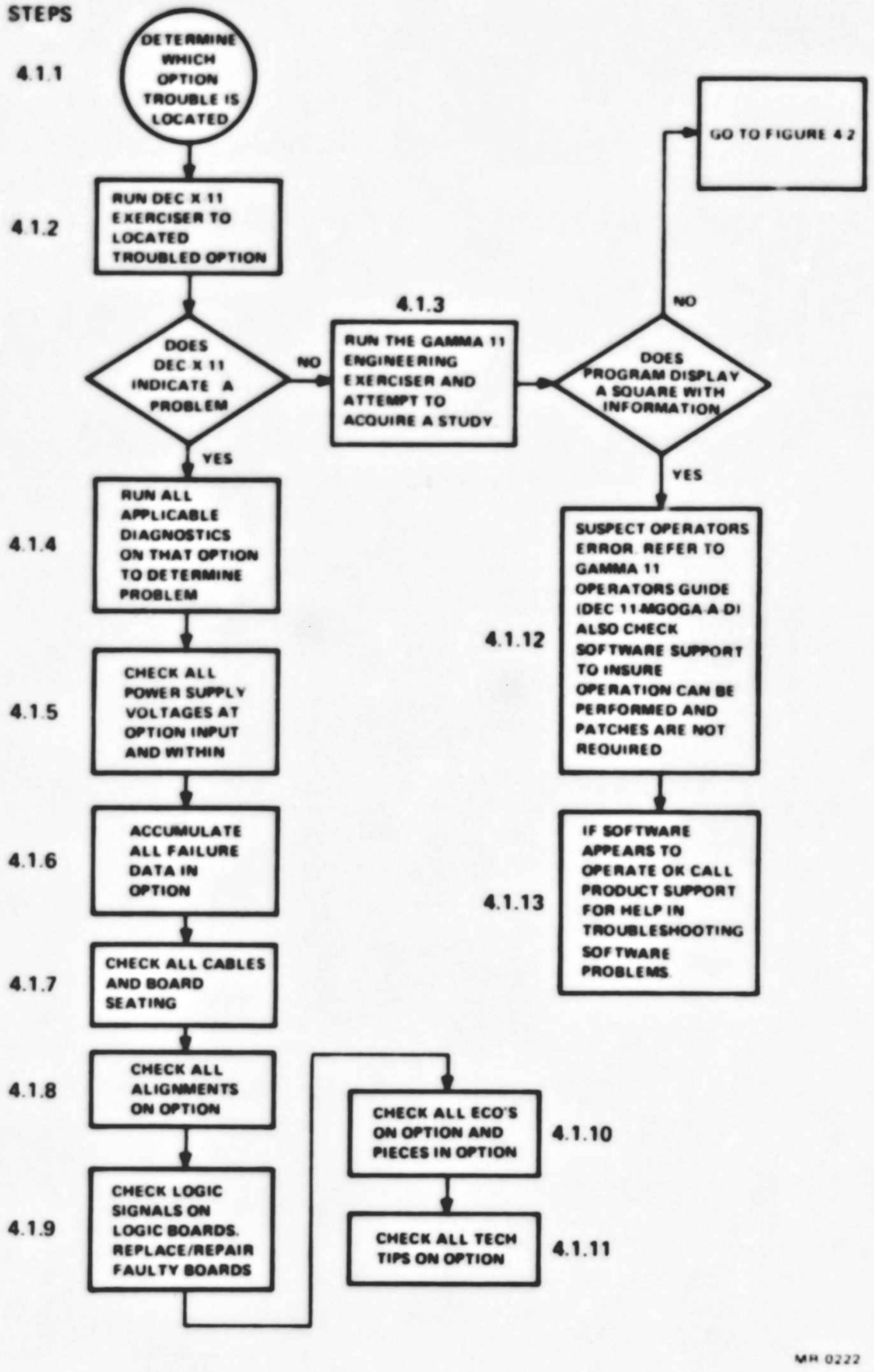

STEPS
4.1.1
DETERMINE WHICH OPTION TROUBLE IS LOCATED
4.1.2
RUN DEC X 11 EXERCISER TO LOCATED TROUBLED OPTION
DOES DEC X 11 INDICATE A PROBLEM
NO
4.1.3
RUN THE GAMMA 11 ENGINEERING EXERCISER AND ATTEMPT TO ACQUIRE A STUDY
DOES PROGRAM DISPLAY A SQUARE WITH INFORMATION
NO
GO TO FIGURE 4 2
YES
YES
4.1.4
RUN ALL APPLICABLE DIAGNOSTICS ON THAT OPTION TO DETERMINE PROBLEM
4.1.5
CHECK ALL POWER SUPPLY VOLTAGES AT OPTION INPUT AND WITHIN
4.1.6
ACCUMULATE ALL FAILURE DATA IN OPTION
4.1.7
CHECK ALL CABLES AND BOARD SEATING
4.1.8
CHECK ALL ALIGNMENTS ON OPTION
4.1.9
CHECK LOGIC SIGNALS ON LOGIC BOARDS. REPLACE/REPAIR FAULTY BOARDS
4.1.10
CHECK ALL ECO'S ON OPTION AND PIECES IN OPTION
4.1.11
CHECK ALL TECH TIPS ON OPTION
4.1.12
SUSPECT OPERATORS ERROR REFER TO GAMMA 11 OPERATORS GUIDE (DEC 11-MGOGA-A-D) ALSO CHECK SOFTWARE SUPPORT TO INSURE OPERATION CAN BE PERFORMED AND PATCHES ARE NOT REQUIRED
4.1.13
IF SOFTWARE APPEARS TO OPERATE OK CALL PRODUCT SUPPORT FOR HELP IN TROUBLESHOOTING SOFTWARE PROBLEMS
MR 0222

Figure 4-1 System Troubleshooting Flowchart

Answer the command "Enter Keyboard Command" with an "F" and the exerciser will acquire data, for a few seconds, then display that data on the VRV01 Color Video Monitor. For time-dependent problems, type the letter "C". This will allow data to be continuously collected until stopped by typing the letter "S". The data collected in this manner can be displayed at any time during collection by typing the letter "D". The displayed data will be an accumulation of all data collected up to the time the "D" key is depressed.

A square with random data should be displayed 5 to 10 seconds after an "F" is typed. The Z count and matrix count data should be viewed on the bottom of the display. If not, run the VSV01 diagnostics to check the display. If the square is displayed without random dots, run the NC11-A logic test and check the NC11-A timing. Once the timing is set and the logic test as run successfully, rerun the Gamma-11 exerciser.

The Z count represents all the Z pulses that are accepted by the NC11-A while the matrix count represents all the valid counts accepted into memory. Therefore, the Z count and matrix count will not always be equal. The matrix count will often be lower than the Z count because of the following.

1. The information at the input of the A/D converters are out of range and, therefore, not converted. Signal less than 0 volt or greater than 4 volts as measured at the output test point are out of range.

2. The cells reach maximum count and, therefore, additional counts in these cells are disregarded.

4.1.4 - 4.1.11 Option Checkout

Follow steps 4.1.4 through 4.1.11 thoroughly. Run all the diagnostics. If the Gamma-11 Exerciser collects data, an error may occur in the List Mode operation, or Matrix Mode resolution. Check the characteristics of the Z pulse. Refer to Chapter 5, Address Maker for more detailed information. The LSB bit from the NAD01 converter should be checked using a scope. This problem of incorrect Z pulses from the Gamma Camera will not occur when running the Gamma-11 Exerciser.

4.1.12 and 4.1.13 Software/Operators Errors

If all above has been accomplished and a problem persists, follow step 4.1.13. Request additional information from Product Support if a problem still exists.

4.2 NC11-A/NAD01 TROUBLESHOOTING

The following paragraphs provide information related to troubleshooting the NC11-A Interface and the NAD01 A/D Converters. Each paragraph number corresponds to each step number presented in the flow chart illustrated in Figure 4-2.

4.2.1 NC11-A Problems

NC11-A Interface failures may be caused by the following.

1. NC11-A Logic Failures
2. NAD01 A/D Converter Logic Failure
3. Misalignment of the NC11-A or NAD01 Logic (see Paragraph 4.3)
4. Operator Error

To determine or isolate existing failures it is recommended to perform the following.

1. Check power supply outputs.
2. Ensure that all cable connectors and circuit board are seated properly.
3. Check input pulses from camera, the timing and alignment.
4. Ensure that all the latest ECOs and TECH tips have been incorporated.
5. Load and run logic engineering diagnostics.

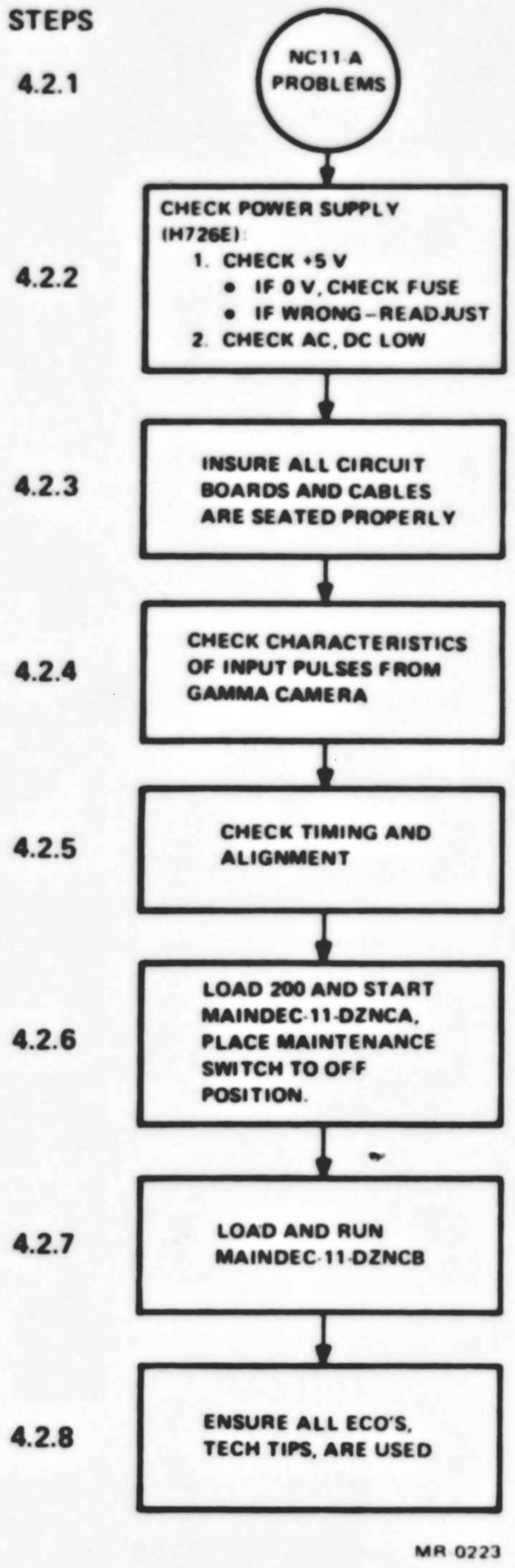

STEPS
4.2.1
NC11-A PROBLEMS
4.2.2
CHECK POWER SUPPLY (H726E):
1. CHECK +5 V
• IF 0 V, CHECK FUSE
• IF WRONG—READJUST
2. CHECK AC, DC LOW
4.2.3
INSURE ALL CIRCUIT BOARDS AND CABLES ARE SEATED PROPERLY
4.2.4
CHECK CHARACTERISTICS OF INPUT PULSES FROM GAMMA CAMERA
4.2.5
CHECK TIMING AND ALIGNMENT
4.2.6
LOAD 200 AND START MAINDEC-11-DZNCA, PLACE MAINTENANCE SWITCH TO OFF POSITION.
4.2.7
LOAD AND RUN MAINDEC-11-DZNCB
4.2.8
ENSURE ALL ECO'S, TECH TIPS, ARE USED
MR 0223

Figure 4-2 NC11-A Troubleshooting Flowchart

4.2.2 Power Supply Check

The H726E power supply provides operating voltages for the NC11-A and the Unibus (when NC11-A is located at the end of the Unibus). Therefore, problems located in the power supply could effect the system operation as well as the NC11-A. To isolate power supply problems perform the following:

1. Check for +5 V on pin A32A2 of NC11-A backplane. If at 0 V, check fuse and fuse connection in holder on the power supply.

NOTE

Some H726E units contain a paper type fuse holder which can corrode at the terminals causing intermittent operations.

It is recommended to replace the power supply if replacement of the fuse holder does not correct the problem.

2. Adjust the output to +5 V using the potentiometer located on the regulator board.

3. Check the ac and dc low signals from the power supply.

If these signals (one or both) are low, a power or "Hung" system will occur. If either signal is low, remove the "fast on" tabs to the ac and dc low located at the power connector side of the NC11-A logic rack and check the ac, dc low signal on the Unibus (pins B1 F1, B1 F2 of the NC11-A). It is recommended to replace the power supply if both signals are high.

4. Check for ±12 V and ±24 V (±6 V is not used) at the test points located on front of the NIMBIN power rack. Adjust to ±1% using the adjustment at the rear of the NIMBIN rack in the power supply section. This adjustment can be made through the holes in the screen.

4.2.3 Connectors and Module Connections

All cable connectors, cables, and circuit boards should be checked for breaks, cuts, shorts, open circuits. Insure that the circuit boards are seated properly. Insure that all unused inputs to the NAD01 converters have shorting plugs as explained in Chapter 3. In addition, if either ZA or ZB inputs to the NC11-A (located on the NC11-A side panels) are not used, insert a shorting plug.

4.2.4 Gamma Camera Pulse Characteristics

Check the signals from the Gamma Camera. Refer to Chapter 3, Paragraph 3.3 for the proper pulse characteristics for each of the various cameras used in Gamma-11 System. See Table 4-1 for camera signals and test points.

Table 4-1 Camera Signals

Signals	Test Point
ZA	A30R2
ZB	A31R2
X (±X)	X NADDI Input Test Point
Y (±Y)	Y NADOI Input Test Point

4.2.5 Timing and Alignment

Checking the timing of the NC11-A interface is accomplished by running the Gamma Toggle Program (refer to Table 4-2).

Table 4-2 Toggle Program

MOV#100 @# SFR	400: 012737	000100	164014	:Clear Option
MOV#20000 @# OFR	406: 012737	020000	164002	:Load 20000 in offset
MOV#1003 @# CSR	414: 012737	001003	164000	:64 × 64 RES. EN RPR. EN ADC
MOV#24 @# SFR	422: 012737	000024	164014	:Software convert. CLR WC and CA
NOP	430: 000240			
NOP	432: 000240			
BR.-5	434: 000772			:Branch back to 422:

The program does the following.

1. Resets NC11-A Logic
2. Sets offset register to 20,000 (all data collected will be placed in memory without overrunning the toggle program).
3. Sets up 64 × 64 cell resolution and enables the NPRs and A/D converters via the Command Status Register.
4. Clears the Word Count (WC) and Current Address (CA) Registers and performs software conversions, under software control. This triggers the A/D converters and transfers the results into memory.

When operating the Toggle Program the signals from the Gamma Camera (pins ZA and ZB) must be at 0 V and the dc levels at the output tests points (located on front of NAD01s) are set to +2 V (without input). Adjustment and alignment information is presented in Paragraph 4.3.

4.2.6 Load and Run MAINDEC-11-DZNCA

The NC11-A Logic test (MAINDEC-11-DZNCA) can now be run and will check the function of the logic located in the logic rack. The A/D converters must be connected to the NC11-A.

NOTE

It is recommended not to move the connection of the joystick from AR11 to the NC11-A as realignment may be required.

Load MAINDEC-11-DZNCA. Set the switch register to 0, the MAINT switch on the NC11-A to the OFF (down) position and install shorting plugs on ZB and ZA.

Start program at 200. The first pass does a minimum number of iterations which takes approximately 30 to 90 seconds depending on the processor used. Most "hard" errors will be detected on the first pass. Additional passes will take approximately five minutes.

The NC11-A logic can be considered operational after two passes have been completed without detecting an error. This test should run error free for at least twice as long as the average time between failures for intermittent problems.

4.2.7 Load and Run MAINDEC-11-DZNCB

The Gamma-11 Exerciser (MAINDEC-11-DZNCB) can now be run. This will check the NAD01 A/D converters. In addition, this program is used when adjusting the converters. Refer to Paragraph 4.3 for adjustment procedure.

4.2.8 Review Latest ECOs and Tech Tips, and Change Notices

It is extremely important that all latest ECOs and Tech Tips for all Gamma-11 options and Change Notices for the MAINDEC-11 diagnostic programs are reviewed and incorporated. Intermittent or solid failures may result if latest ECOs are not incorporated. In addition, only the latest revision of diagnostics should be used.

4.3 ADJUSTMENT AND ALIGNMENT

The following paragraphs present the recommended information required to align and adjust the following.

1. Power supply
2. NC11-A Interface
3. NAD01s A/D converters
4. Zoom Mode adjustment
5. Joystick

4.3.1 Power Supply

All required adjustments to the H726E and NIMBIN power supplies are listed in Table 4-3. Adjustments should be made using a digital voltmeter.

Table 4-3 Power Supply Adjustments

Voltage	Tolerance	Pin Number	Ripple	Adjustment
+5 V		A32A2 (NC11A Backplane)	20.0 mV (max) Peak-to-Peak	Potentiometer on Regulator board
±12 V	±1%	Test Points Front of NIMBIN Power Rack		Potentiometer through screen at the rear of of the Power Supply
±24 V	±1%	Test Points Front of NIMBIN Power Rack		
±6 V	-	-		Not used

4.3.2 NC11-A Interface

The adjustment and alignment of the NC11-A Interface is accomplished with aid of the Gamma Toggle Program (see Table 4-2).

When operating this program the signals from the Gamma Camera on pin ZA and ZB must be at 0 volts. The dc levels at the output test points (front of the NAD01's) must be set at +2 volts (without inputs). Adjust the offset potentiometer if this voltage is not correct.

The information required to align the NC11-A is listed in Table 4-4. The following paragraphs present an explanation of each signal listed in Table 4-4.

D04 TEST CLK - This signal has a continuous string of 50-ns pulses occurring at a 10 μs rate. Adjust the potentiometer located on the M401 (Slot B31) if out of tolerance by more than ± 10%. This signal being out of tolerance may result in failure of the DEC X-11 Exerciser.

D10 CLEAR WC + CA H - This signal is adjusted to a 1.0 μs ±5% pulse width. When an overflow condition occurs, an interrupt, if enabled will be generated. Once serviced, the overflow and the WC and CA Registers are cleared by D10 CLEAR WC + CA H.

D11 RIP DEL H - This signal is generated at the end of the read NPR cycle to allow time for the matrix data to be incremented and checked for an increment overflow. At the end of the RIP Delay the second or write NPR cycle will be canceled if an incremented overflow occurs and the data for that matrix element will remain at its highest count.

Table 4-4 NC11-A Alignment

Signals	Location	Slot No.	BD No.	Pulses
D04 TEST CLK L	B31E2	B31	M401	10 μs period
D10 CLEAR WC + CA H	B27T2 Bottom	B27	M302	1 0 μs pulse width
D11 RIP DEL H	B27F2 Top	B27	M302	400 ns pulse width
D04 COINC DEL H	B25T2 Bottom	B25	M302	150 ns pulse width (min)*
D04 COINC H	B26T2 Bottom	B26	M302	0.5–1.0 μs pulse width
D04 CLEAR ADC H	B25F2 Top	B25	M302	250 ns pulse width (min)*
D04 DEAD TIME H	B26F2 Top	B26	M302	5–7 μs pulse width

* Or minimum pot setting.

NOTE

These are initial settings and may need to be changed slightly for optimum operation. The delay settings are dependent upon front end electronics and are adjustable to provide signal timing compensation.

D04 COINC DEL H - This signal delays the NC11-A allowing the analog pulse from the Gamma Camera to be sampled at the proper time and amplitude. This signal should be adjusted so that the COINC pulse occurs at the earliest point in time where the X and Y data, as seen at the output test points, (see Figure 4-3) has reached a stable plateau level.

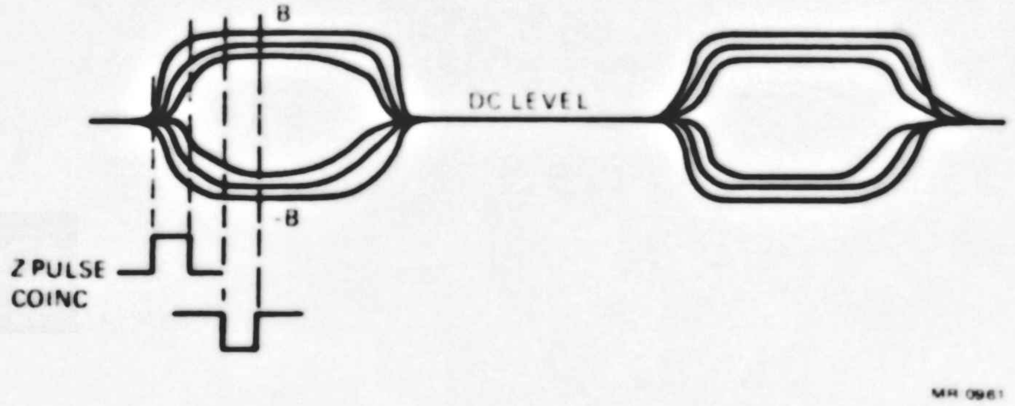


Figure 4-3 NAD01 Control Adjustments

D04 COINC H - The COINC pulse width determines the length of time the NAD01 A/D converters will sample the analog pulse from the camera. If the length is short, the converters will not sample long enough; if too long, the converters will sample after the analog pulse returns to its dc level allowing a "hot" area on the display.

The COINC pulse width should be adjusted to a minimum value in the range of 500 ns to 1.0 μs without the presence of artifacts (hot spot on display).

D04 CLEAR ADC H - This pulse clears the converters. When setting the timing on this one-shot, the half voltage points should be used for reference (minimum pot setting but not less than 250 ns).

D04 DEAD TIME - The Dead Time one-shot inhibits additional Z pulses from entering the NC11-A Control Logic while the NAD01s are converting. This signal should be adjusted to the minimum value of the 5 to 7 μs range that allow reliable operation.

4.3.3 NAD01 A/D Converters

Perform the following procedure to adjust the NAD01 converters.

1. Set the Gamma Camera's output to 30,000 counts per second with flood source or remove the collimator and place a radioactive source approximately two to four feet from the camera's crystal. It is recommended that the camera operator performs this task.
2. Set the oscilloscope to 1 volt/div vertical input and the time base to 2 μs/div.
3. Attach the scope probe to the OUTPUT test point of the X or Y NAD01 A/D converter. Adjust the offset potentiometer (front of converter) so the dc level is 2 V as shown in Figure 4-3.

4. Adjust the GAIN 2 potentiometer so that the maximum and minimum of the envelope of data pulses depicted in Figure 4-3 as B and −B correspond to 4 V and 0 V, respectively.

NOTE

These 10- to 22-turn potentiometers may require many turns before a change is noted.

If an output is not present at the OUTPUT test point (front of converter), check the INPUT test point. Replace the NAD01 converter if a signal is present at the INPUT test point. If this signal is not present (at the INPUT testpoint) disconnect signal cables from the camera and verify that a signal is present. If the signal is present, the NAD01 converter could be faulty or the output signal from the camera is not sufficient to drive the NAD01 input.

Once the GAIN and OFFSET adjustments on both converters are completed, load Gamma-11 Exerciser (MAINDEC-11-DZNCB) and start at 200. Type an "F" which causes data to be collected and displayed on the VRV01. A symmetrical circle or hexagon should be displayed in the center of the display box as depicted in Figure 4-4. If it is not symmetrical (side cut off), adjust the GAIN 2 and OFFSET potentiometers on the converters until a full picture is displayed. If "Hot Spots" occur, adjust the COINC and COINC DELY in the NC11-A Interface.

For circular outlines, the edge of the display should touch each side of the box as depicted in Figure 4-4a. If an hexagonal outline is displayed, the left and right points should touch the left and right side of the box. (See Figure 4-4b). If not, adjust GAIN 2 and OFFSET potentiometers so that A and B (Figure 4-4b) are equidistant.

Now check the Gamma Camera display with the VSV01 display by placing a point source (with collimator installed) at the upper left position of the camera face. Verify that the point source is in the same position on both displays as illustrated in Figure 4-5. If not, ensure that all orientation switches are properly set up. If the point source is inverted on the display and individual cables are used for the X and Y signals, change the cables from + input to − input. When two cables per signal are used, invert the cables.

4.3.4. Zoom Mode

The following procedure is recommended to set the GAIN Controls for the Zoom mode. This is adjusted using the MAINDEC-11-DZNCB program. Start the program at 200 and type F.

1. Set the SCALING AMP switches to VARIABLE and reduce the display diameter to 1/2 the original size with the VARIABLE GAIN knob. Be sure this display is the same uniform shape as the original.

NOTE

The amount of reduction done during the variable gain adjustment is inversely proportional to the resultant magnification. That is, if the display were reduced to 2/3, the resultant image would be 3/2 = 1.5 times the original image. Some customers may wish to have other than 2:1 setting. Some limitations are also imposed by the input signal magnitude from the camera.

2. Switch to zoom mode in the exerciser by typing "Z" and adjust GAIN 1 to present the original large size image. The shape of the image is more important than the size.

3. Set the SCALING AMP switches to UNITY. A 2X view of the center of the original image should be displayed.

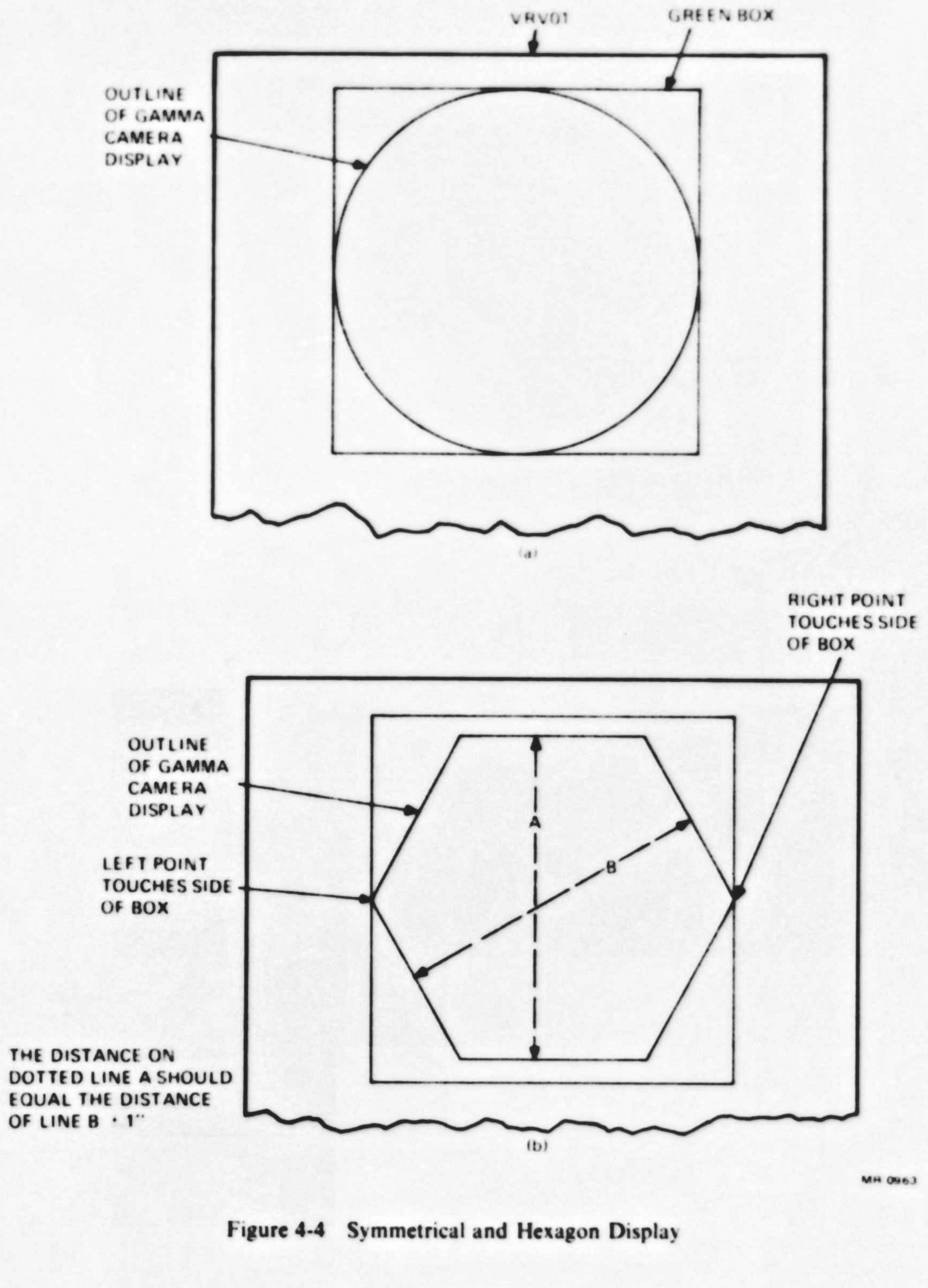

VRV01
GREEN BOX
OUTLINE OF GAMMA CAMERA DISPLAY
(a)
RIGHT POINT TOUCHES SIDE OF BOX
OUTLINE OF GAMMA CAMERA DISPLAY
A
B
LEFT POINT TOUCHES SIDE OF BOX
THE DISTANCE ON DOTTED LINE A SHOULD EQUAL THE DISTANCE OF LINE B · 1"
(b)
MH 0963

Figure 4-4 Symmetrical and Hexagon Display

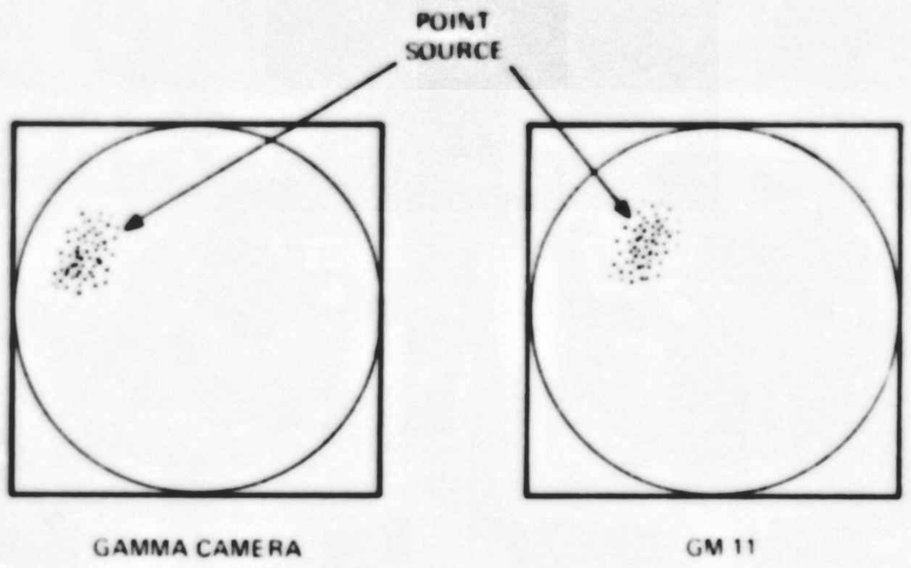


Figure 4-5 Position of Point Source

4.3.5 Joystick

The following is a procedure to adjust the H306 joystick for the AR11 and NC11-A configurations. The GAMMA-11 Exerciser (MAINDEC-11-DZNCB) should be running.

1. AR11 Configuration

   a. Type letter "J"

   b. Adjust the X and Y potentiometers (on the H306) so that the "dot" (VT01) or cross hairs (VSV01) provide uniform access within the box displayed on the screen.

      NOTE

      Ideally, the physical center of the joystick should provide a point displayed approximately centered in the box.

   c. Ensure that the display point does not follow the joystick when the joystick interrupt bar is depressed.

   d. A "CNTRL C" will return the user back to the keyboard monitor of the exerciser.

2. NC11-A Configuration

   a. Type letter "K"

   b. Repeat step 1-b above. The X and Y EXT GAIN controls on the NAD01 converters may require adjustment to realize this step.

      NOTE

      The A/D converter must be properly aligned. If not, the NC11-A no convert flag will set as indicated by the ringing of the bell on the printer. (A "CNTRL G" will turn OFF/ON the bell.)

   c. Repeat step 1-c above.

   d. Repeat step 1-d above.

CHAPTER 5

CHAPTER 5
DETAILED THEORY OF OPERATION

The NC11-A option is designed to interface a Gamma Camera and a PDP-11 computer in the Gamma-11 Nuclear Medicine System (see Figure 5-1). (Refer to document EK-NC11A-TM for a general description.) The following paragraphs present a detailed description of each circuit of the NC11-A as shown in Figure 5-2 and presented in the NC11-A Engineering Drawings (see Table 5-1).

5.1 COMMAND AND STATUS REGISTER (Drawing Number NC11-A-03)

The Command and Status Register (CSR) controls and monitors operation of the NC11-A. This register is loaded with the desired operation after all other registers have been initialized to their desired values; for example, Word Count, Current Address and Offset Registers should be initialized before the CSR. The CSR is cleared by reset. See Tables 5-2 and 5-3 for the bit assignments in this register.

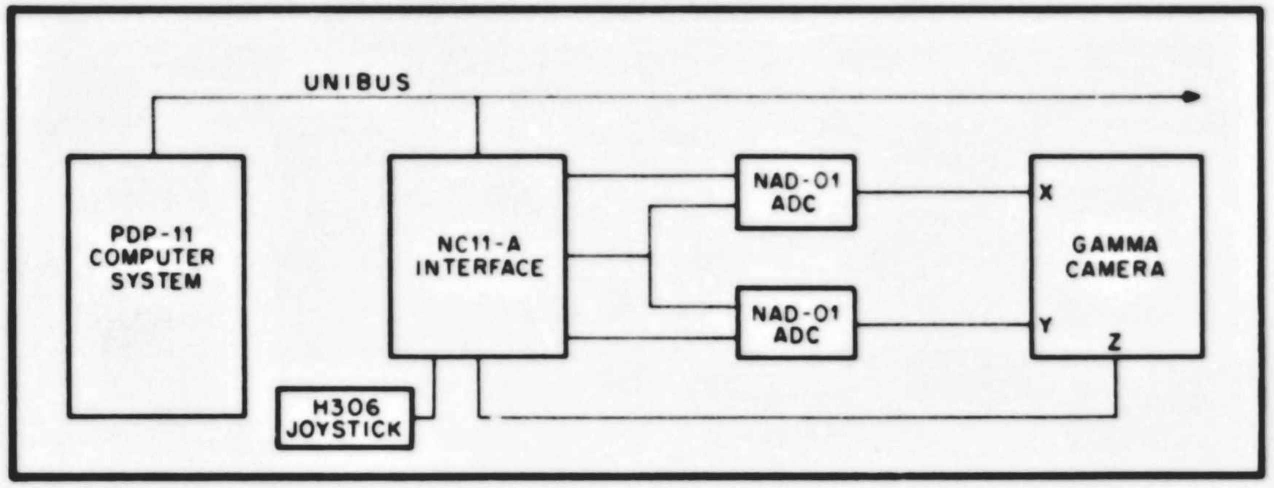

UNIBUS
PDP-11 COMPUTER SYSTEM
NC11-A INTERFACE
NAD-01 ADC
NAD-01 ADC
X
Y
Z
GAMMA CAMERA
H306 JOYSTICK
MR-0964

Figure 5-1 System Block Diagram

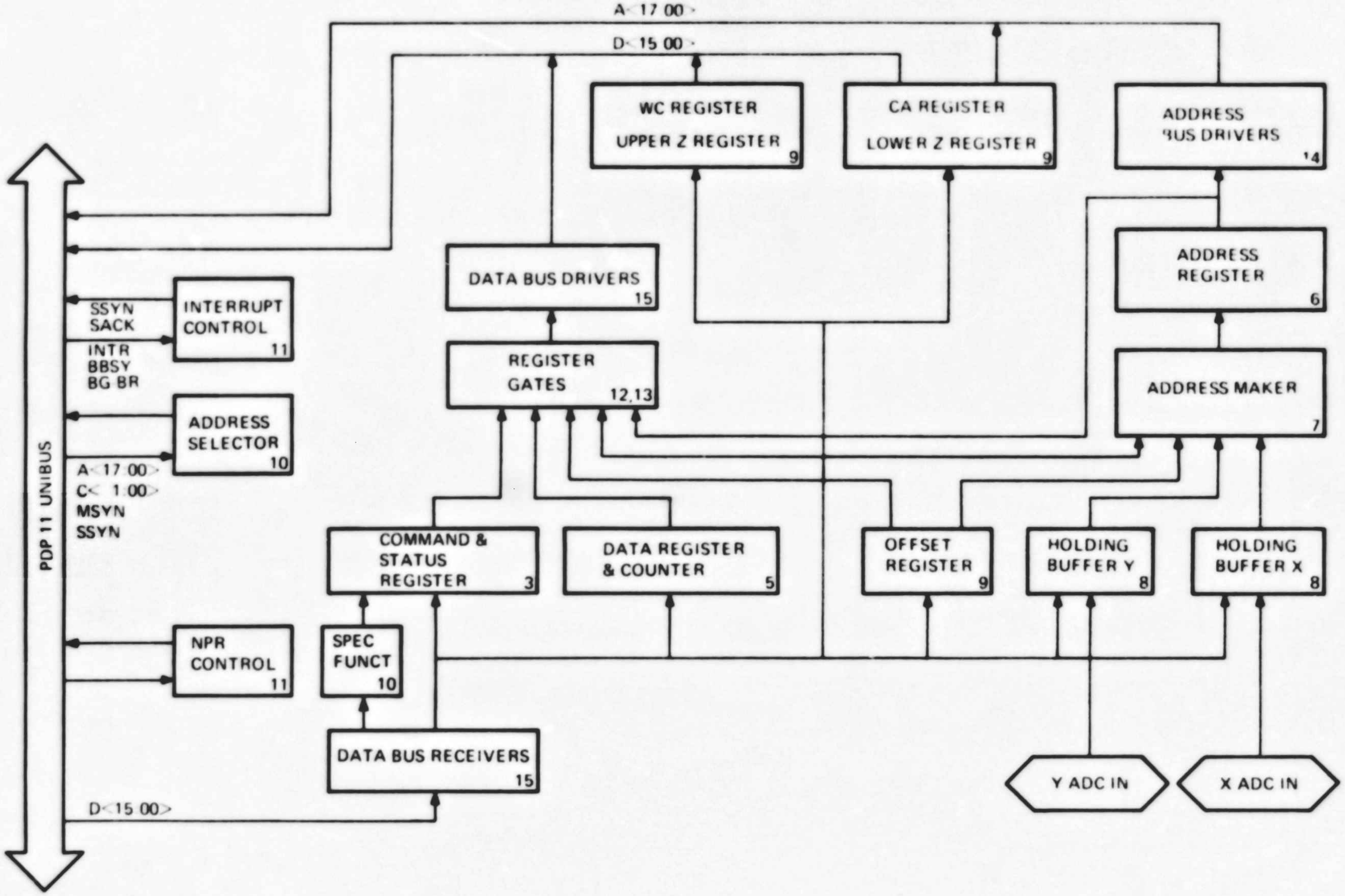

A<17:00>
D<15:00>
WC REGISTER
UPPER Z REGISTER
9
CA REGISTER
LOWER Z REGISTER
9
ADDRESS
BUS DRIVERS
14
ADDRESS
REGISTER
6
ADDRESS MAKER
7
DATA BUS DRIVERS
15
REGISTER
GATES
12,13
SSYN
SACK
INTR
BBSY
BG BR
INTERRUPT
CONTROL
11
ADDRESS
SELECTOR
10
A<17:00>
C<1:00>
MSYN
SSYN
PDP 11 UNIBUS
COMMAND &
STATUS
REGISTER
3
DATA REGISTER
& COUNTER
5
OFFSET
REGISTER
9
HOLDING
BUFFER Y
8
HOLDING
BUFFER X
8
NPR
CONTROL
11
SPEC
FUNCT
10
DATA BUS RECEIVERS
15
D<15:00>
Y ADC IN
X ADC IN
MR 0973

Figure 5-2 NC11-A Block Diagram

Table 5-1 Drawing List*

Drawing Number*	Title
NC11-A-03	Command and Status Register
NC11-A-04	Control Logic
NC11-A-05	Data Register
NC11-A-06	Address Register
NC11-A-07 (Sheets 1 through 3)	Address Maker
NC11-A-08	X and Y Hold Registers
NC11-A-09	Offset WC, CA, Z Registers
NC11-A-10	Address Select Special Function
NC11-A-11	Nonprocessor Request (NPR) Control
NC11-A-12	Command and Data Register Gating to Bus
NC11-A-13	Address and Offset Gating to Bus
NC11-A-14	Address Register Output Gating Driver
NC11-A-15	Unibus Receivers and Drivers

* Located in NC11-A Engineering Drawings

Table 5-2 Command Register (Read-Write)

Bit	Name	Function
0	HNPR	Enables the interface to perform an NPR cycle. This bit must be set for Matrix and List Mode and is not set for Joystick Mode.
1	ENABLE ADC	Enables the A/D converters. This bit must be set for Matrix, List and Joystick Modes of operation.
2	LIST MODE	This is set for List Mode only. Default is Matrix or Joystick Mode.
3	JOYSTICK MODE	This bit is set for Joystick Mode and will inhibit NPR cycles.
4	EXT	This bit causes a relay in the A/D converters to connect the EXTERNAL INPUT to the A/D converter. This bit must be set in Joystick Mode if the joystick is connected to the NAD01 A/D converter.
5	GAIN	This bit causes a relay in the A/D converter to switch from GAIN 2 (Standard) to GAIN 1 (Zoom Mode).
6	ENAB OVFL INT	Enables interrupt to vector 270 on a cell overflow. (256 in Byte Mode, 65,536 in Word Mode).
8-10	RESOLUTION	Select the resolution for Matrix Mode of data collection. 000 NOP 001 LIST MODE 010 64 × 64 × 16 (word) 011 32 × 32 × 16 (word) 100 128 × 128 × 8 (base address = 0) 101 128 × 128 × 8 (base address = 4 K) 110 64 × 64 × 8 (byte) 111 32 × 32 × 8 (byte)
11	ENAB Z OVFL INT	Enables interrupt on Z COUNT or WORD COUNT overflow to vector 274.

Table 5-3 Status Register

Bit	Name	Function
7	BUSY/DONE	This bit is set by the Special Function Register signal CONV and cleared at the completion of the conversion. The use of this bit is confined to joystick mode.
12	Z/WC OVERFLOW	Set when Z or WORD COUNT overflow in Matrix or List Mode, respectively; this bit will cause interrupt to vector 274 if bit 11 of the CSR is set.
13	INCR OVERFLOW	Set if data cell overflows during increment. This bit will cause an interrupt to vector 270 if bit 6 of the CSR is set.
14	NO CONV	Set to a one if the A/D converters fail to convert a signal within the time specified by the dead time delay.
15	TIME OUT/JOY DEP	Set if a NPR time out occurs when addressing a memory that does not respond. Set also by the joystick "interrupt" bar or the remote start switch.

5.2 CONTROL LOGIC (Drawing Number NC11-A-04)

The control logic is initialized by the Command Register to provide the appropriate interaction between asynchronous signals from the camera, A/D converter and the PDP-11 Unibus. The control logic provides three levels of data buffering that is common to Matrix, List and Joystick modes of operation. The three data buffers are as follows.

1. ADC Output Buffer in the NAD01
2. X-Y Hold Register
3. Address Register

As depicted in Figure 5-2, the data flows from the ADC Output Buffer to the X-Y Hold Register; from the X-Y Hold Register through the address maker to the Address Register, and from the address register to the Unibus address lines for Matrix Mode; or to the Unibus data lines for List and Joystick Modes. The flow of data is controlled by the three control flip-flops labeled ADC FULL (COORD D7•), HOLD FULL (D4•), and ADD FULL (D1). Each control flip-flop sequences the data to the next register automatically as soon as it becomes empty. The ADD FULL flip-flop holds the data in the Address Register until the NPR DONE signal (indicates both read and write NPR cycles done) occurs in Matrix Mode; until the end cycle signal occurs in List Mode; and until the Address Register is read (RD ADD REG) in Joystick mode.

The HOLD FULL flip-flop holds data in the X-Y Hold Register until the Address Register is available and the ADC FULL flip-flop holds the data in the ADC output buffer until the X-Y Hold Register is available. If all three registers become full, A/D conversions are inhibited until transfer between registers clears the ADC FULL flip-flop.

The ADC FULL flip-flop inhibits CLEAR ADC via NAND gate (M113) B23N2 coordinates C5. Under normal operation, the three registers should not be full. A full condition indicates a logic problem in the control of NPR circuits or Bus Latency problems.

• Refers to location in Drawing NC11-A-04, Print Set.

5.2.1 Matrix Mode Operation

In Matrix Mode the interface takes the results of the X and Y A/D converters stored in the X-Y Hold Register, combines this data with content of the Offset Register and Extended Memory Bits to produce an address. Each such address of the matrix corresponds to a physical element on the surface of the camera; for example in 64 × 64 × 16 Matrix, the surface of the camera is divided into 64 X and 64 Y elements giving 4096 total discrete elements. When a particular element detects a photon due to a gamma ray striking the camera crystal, a Z pulse is generated, and the X and Y analog signals correspond to the effective address of this element. The content of the address is read by the interface using an NPR cycle into the Data Register, incremented, and if no overflow occurs the interface performs a write NPR cycle to store the incremented value. In this manner a three-dimensional array is built up in memory of X, Y, and counts per element. If a cell overflow occurs, the write NPR cycle is canceled so that the data remains all ones.

Matrix data is collected in several selected manners.

1. Fixed Time – The interface collects data until stopped by a real-time clock routine at the desired time.
2. Matrix Cell Overflow – The interface collects data until a cell overflows and stops operation.
3. Fixed Z Count – NC11-A collects data until a fixed Z count is reached.
4. Combination of Fixed Time and Matrix Cell overflow.
5. Combination of Fixed Z Count and Matrix cell overflow.

NOTE

In Matrix mode the CA and WC registers are connected to form a 32-bit Z COUNT Register. Each time COINC DEL triggers, the CA is incremented by signal COUNT CA. Each time CA OVFL occurs the WC Register is incremented by signal COUNT WC (Coordinates C2).

After proper initialization via the Control Register, the following signals will be true.

Signal	**Coordinates**	**Function**
HNPR (1)	C8, A8	Enable NPR
ENA ADC (1)	D8, C6	Enable ADC
MAINT SW OFF	C8	Disable Test CLK
RESOLUTION		(Selected Resolution)

The interface will conditionally be set to stop on Z overflow, cell overflow, or by clearing HNPR at fixed time with any desired interrupts enabled.

A Z pulse from the camera starts operation of the interface. The Z pulse may be from either the A or B isotope and is received by M501 Schmitt triggers. The Z pulse must meet the requirements as depicted in Figure 3-7.

The output of the M501s are gated by the REJECT L signal which disables Z pulses for the following reasons.

SIGNAL	MEANING
D04 ADC FULL (1)	All 3 Data Registers are full
D03 Z/WC OVFL (1)	Z Count overflow
DEAD TIME (1)	The fixed "Dead Time" of the NC11-A is in effect.

The gated Z pulse sets the COINC DELAY One-Shot and in turn the COINC H One-Shot. Each of these delays is adjustable. The COINC DELAY is adjusted to set the COINC H signal in the plateau region of the X and Y data signals as seen at the output test point of the respective NAD01 converter. The COINC pulse width is adjustable from 0.5 to 1.0 μs to meet the Coincidence width required by the A/D converter to obtain a valid sample. CON L (coordinates C1) is sent to the A/D converters to start an A/D conversion. The X and Y data are sampled while the pulse is low and the conversion is initiated on the trailing edge of the negative pulse. The gated Z pulse also sets the DEAD TIME one-shot (5–7 μs). The DEAD TIME flip-flop (coordinates B1) was previously set by the "OR" of the Z pulses D04 Z PULSE L. The DEAD TIME flip-flop inhibits additional Z pulses until the DEAD TIME One-Shot clears the flip-flop on its trailing edge.

The interface must now wait for the A/D converters to perform the conversion. Both A/D converters must convert a valid signal (0–4 volts at the output test point). X, Y signals out of range will not convert and the A/D converters will be cleared at the end of the DEAD TIME delay via signal DEAD TIME DLY (coordinates C6). For in-range signals the X STORE and Y STORE signals (coordinates D8) will become true when the converted data is available. The "AND" of these signals triggers an M606 pulse amplifier that directly sets the ADC FULL flip-flop.

ADC FULL (1) is "ANDed" with HOLD FULL (0) which triggers an M602 pulse amplifier LD HOLD L and in turn LD X H and LD Y H when the X-Y hold register is available. Signal LD HOLD L clears the ADC FULL flip-flop on its trailing edge. The X-Y data from the A/D converters resides in the X-Y HOLD registers at this point in time and the D04 HOLD FULL (1) is set. LD HOLD also triggers the CLEAR ADC one-shot (coordinates C5), that clears the ADCs for the next data conversion.

HOLD FULL (1) is "ANDed" with Z/WC OVERFLOW (0) and ADD FULL (0) to trigger the M602 pulse amplifiers CLR ADD L and LD ADD STB L. CLR ADD L clears the Address Register. LD ADD STB L gates the X-Y Hold Register through the Address Maker gates into the Address Register and sets ADD FULL (1). LD ADD STB L is also applied to an "AND" gate (coordinates A8) to generate signals D04 REQ NPR and D04 REQ RW. These signals are used by the NPR control (drawing NC11-A-11) to perform the READ NPR and the WRITE NPR. The operation of the NPR control is discussed in Paragraph 5.9.1. To summarize, the data content pointed to by the address register is read, incremented, and written back to the same address, provided that an increment overflow has not occurred. The Control Logic waits for NPR DONE to clear the ADD FULL flip-flop.

At the end of the DEAD TIME One-Shot the DEAD TIME delay M606 pulse amplifier triggers (coordinates B1) resetting the DEAD TIME flip-flop and triggering the Clear ADC One-Shot (coordinates C4).

NOTE

The clear ADC One-Shot is triggered twice, once by LD HOLD and once by DEAD TIME delay unless the two events coincide in which case only one clear pulse occurs.

The interface is now primed to accept the next camera data, and Z pulse.

5.2.2 List Mode Operation – CSR Set to List Mode

The control logic operates in a similar manner to matrix mode with the following exceptions:

1. The Word Count and Current Address registers are used separately as their respective names imply. Word Count increments by one and Current Address increments by 2 for each transfer to memory. This is accomplished by the logic at coordinates C3 which generates D04 Count WC/CA L.

2. Only one NPR cycle is requested; a write cycle generated by D04 REQ NPR and D04 SET REQ (coordinates A6).

   NOTE

   REQ RW (Request Read Write) is NOT generated in List mode.

3. The data in the Address Register is treated as data and is gated to the Unibus Data lines via the ADD REG RD signal generated by the DATA to BUS signal on the NPR Logic drawing during the NPR cycle. Address to Bus during the NPR cycle gates the Current Address Register to the Unibus address lines.

5.2.3 Joystick Mode: CSR Set to Joystick

In some systems the joystick is connected to the A/D Converters using the EXT INPUT. The following discussion describes the control logic operation for these systems.

1. The Z pulse inputs to the control logic are inhibited by signal JOYSTICK (1) causing D04 KILL ZA and D04 KILL ZB (coordinate C5). These two signals disable their respective Z signals.

2. JOYSTICK (1) causes D04 JS (coordinates B7) which is used to enable the appropriate gate of the Address Maker.

3. JOYSTICK (1) inhibits NPR cycles via "NAND" gate M115 (coordinates A8).

The joystick position is determined by causing a special function CONV (BIT2 set in the special function register). Signal D10 CONV L (coordinates B5) causes COINC DEL and DEAD TIME H and sets the BUSY flip-flop in the Status Register (CSR). These signals in turn cause the CON L signal to start the A/D conversion of the joystick data at the EXT INPUT and the DEAD TIME flip-flop to set. The control logic waits for the A/D conversion to be completed. Out of range conversions are cleared by the trailing edge of the DEAD TIME DELAY and will set the NO CONV flip-flop in the CSR. In-range signals return X STORE and Y STORE which cause the data to be transferred to the X-Y Hold Register and then to the Address Register. When the Address Register is loaded the LD ADD STB clears the BUSY/DONE flip-flop in the CSR register to indicate that the conversion is complete and the data can be read from the Address Register.

5.2.4 List Playback Mode and Diagnostics

The Control logic allows operation in a playback mode where data collected in List Mode can be formed into matrices. The interface is set with NPR enabled, ADC's disabled and selected resolution. Signal D08 BUS LOAD XY loads the X-Y Hold Register with the data from the List. This signal enters the control logic at coordinates D5 and causes NPR cycles in the same manner as Matrix Mode operation. This mode of operation is used by the Logic Test Diagnostic to verify data paths and NPR operation. In the diagnostic mode, the Maintenance switch is set in the "ON" position, the M401 test CLK can be enabled to cause NPR cycles at a 100 kHz rate. This switch is used when running DEC-X-11 tests.

5.3 DATA REGISTER (Drawing No. NC11-A-05)

The Data Register consists of two M238 Counter Modules. This 16-bit register is used as an increment register and only operates for the Matrix Mode. Its operation depends on the resolution selected in the CSR. All 16-bits are used as an increment counter in word mode. The data contents of the matrix address are loaded into the register by the signal D10 LD I during the Read portion of the NPR cycle.

Signal D11 DATA STROBE causes an increment on each Read NPR cycle. If the increment causes LEFT CARRY, indicating an overflow from all one's to zero, the OVERFLOW STOP signal (refer to NC11-A-04) will set the INCR OVFL flip-flop in the CSR. In addition, INCR OVFL (1) H will cancel the WRITE NPR cycle allowing the contents of the selected address to remain all ones.

The Data Register is divided into a right and left byte of 8 bits each when in the byte mode. Each of the 8-bits corresponds to the low and high byte of the address selected by ADDR 00. Each byte is incremented independent of the other byte. If the content causes either a left or right carry (count = 256_8) the D04 OVERFLOW STOP signal will be generated, as in word mode, thus setting the INCR OVFL flip-flop in the CSR and canceling the Write NPR cycle. The Data (Increment) Register is a Read/Write Register at address 764012 with access for maintenance purposes only.

5.4 ADDRESS REGISTER (Drawing No. NC11-A-06)

The Address Register, consists of a 16-bit register which provides the third level of buffering on the NC11-A. Information from the X and Y Hold Registers is loaded into the Address Register through the Address Maker.

The output of the Address Register is used when the NC11-A is either in the Matrix mode or List mode. If in the Matrix mode, the Address Register loads the address lines of the Unibus and transfers memory data to the Data Register.

In the List mode, the Address Register contains the digital conversion from the NAD01s rather than an address. The left byte contains the Y conversion and the right byte contains the X conversion. This information is then loaded onto the data lines of the Unibus through thhe register gates. This data also includes bit 15 (timing mark). This bit is a software function and is set only by bit 5 in the Special Function Register (Address 164014). Bit 7 of the Address Register will set if an input to the B Gamma Isotope Input receives a pulse. The current Address Register will control the address of this data (Address 164010).

5.5 ADDRESS MAKER (Drawing No. NC11-A07, Sheets 1 through 3)

The Address Maker, provides the function of loading the Address Register with information from the X and Y Hold Registers. Bits 00 through bit 05 are depicted in Sheet 1; bits 06 through bits 11 on Sheet 2; and bits 12 through 15 presented on Sheet 3.

In List mode, the Address Maker passes data, unmodified, from the X-Y Hold Register to the Address Register.

In Matrix mode, the Address Maker makes an address from the Offset Register, B-Gamma bit, and the X-Y values in the Hold Register. Which bits of X and Y are taken depends on the size of the matrix used to collect the data. Matrices which may be specified are as follows.

Matrix	Size
32 × 32 byte	0.5K words
32 × 32 word	1K words
64 × 64 byte	2K words
64 × 64 word	4K words
128 × 128 byte	8K words

Examples are depicted in Figure 5-3, Sheets 1 and 2. The actual formation of an address within these matrices is illustrated in Figures 5-4 through 5-11.

The Offset register is capable of defining the start of any 512-word sector from the start of the second 4K memory stack through the end of memory in units of 512 words. This enables buffering so that one matrix may be dumped from memory to a high-speed device while a new matrix is being filled.

The Address Maker is controlled by the D04 LD BUS signal when the NC11-A is in the List mode. (See Figure 5-12.) Each bit from the X, Y Hold Registers will load into the corresponding bits of the Address Register. (Example; bit 00 of the X Hold Register will locate at bit 00 of the Address Register.)

The Address Maker operates in a similar manner while the NC11-A is in the Joystick mode. However, the B-Gamma signal (bit 07) and the TIME Mark (bit 15) are not used, and therefore grounded.

When the NC11-A is in the Matrix mode, the offset register operates in conjunction with the X and Y Hold Registers to provide a unique address in memory to the Address Register.

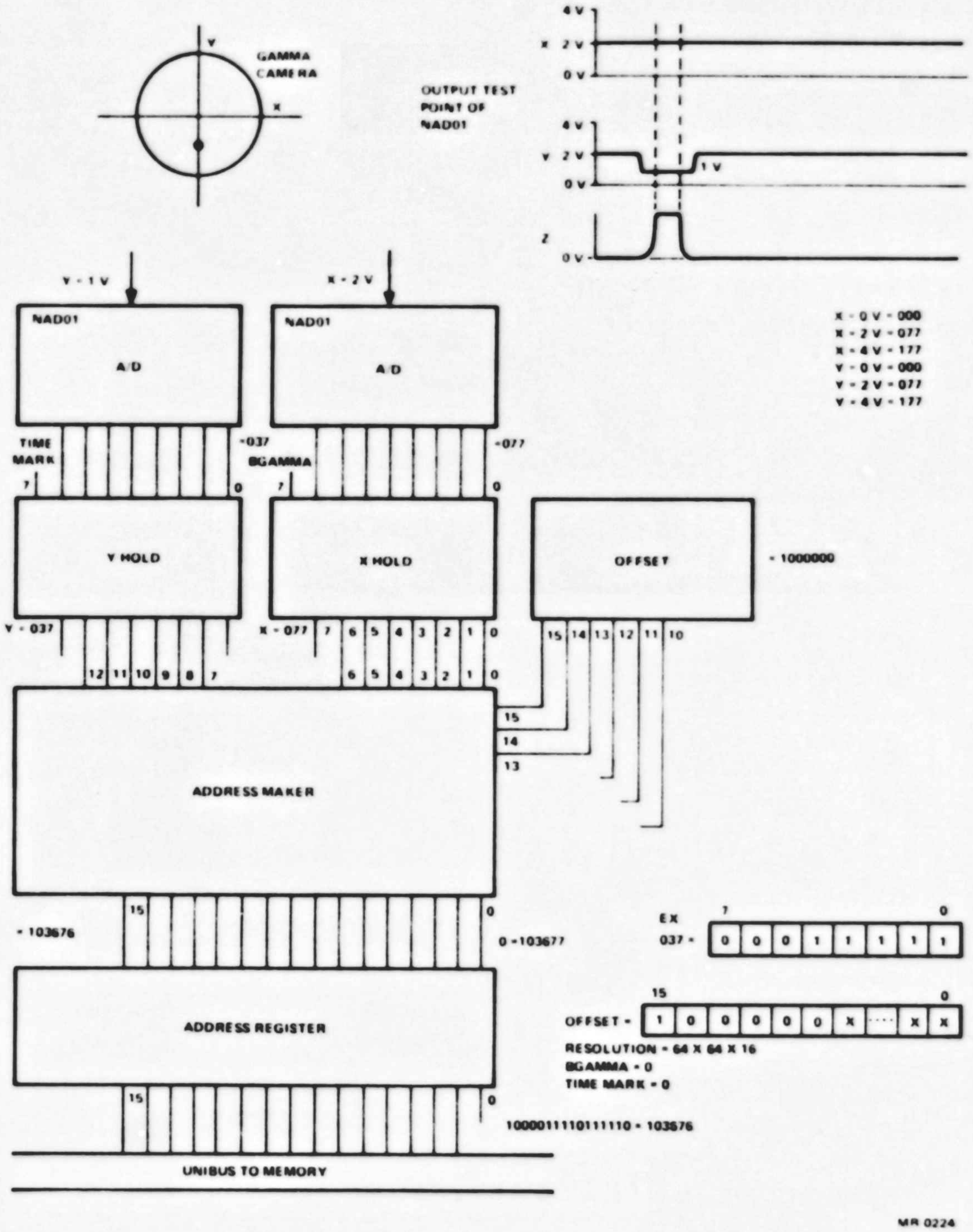

Y
GAMMA
CAMERA
X
OUTPUT TEST
POINT OF
NAD01
4 V
X 2 V
0 V
4 V
Y 2 V
0 V
1 V
Z
0 V
X = 0 V = 000
X = 2 V = 077
X = 4 V = 177
Y = 0 V = 000
Y = 2 V = 077
Y = 4 V = 177
Y = 1 V
X = 2 V
NAD01
A/D
NAD01
A/D
TIME
MARK
7
=037
0
BGAMMA
7
=077
0
Y HOLD
X HOLD
OFFSET
= 1000000
Y = 037
X = 077
7 6 5 4 3 2 1 0
15 14 13 12 11 10
12 11 10 9 8 7
6 5 4 3 2 1 0
15
14
13
ADDRESS MAKER
= 103676
15
0
0 =103677
ADDRESS REGISTER
15
0
1000011110111110 = 103676
UNIBUS TO MEMORY
EX
037 =
7
0
0 0 0 1 1 1 1 1
15
0
OFFSET =
1 0 0 0 0 0 X ···· X X
RESOLUTION = 64 X 64 X 16
BGAMMA = 0
TIME MARK = 0
MR 0224

Figure 5-3 Address Maker (example) (Sheet 1 of 2)

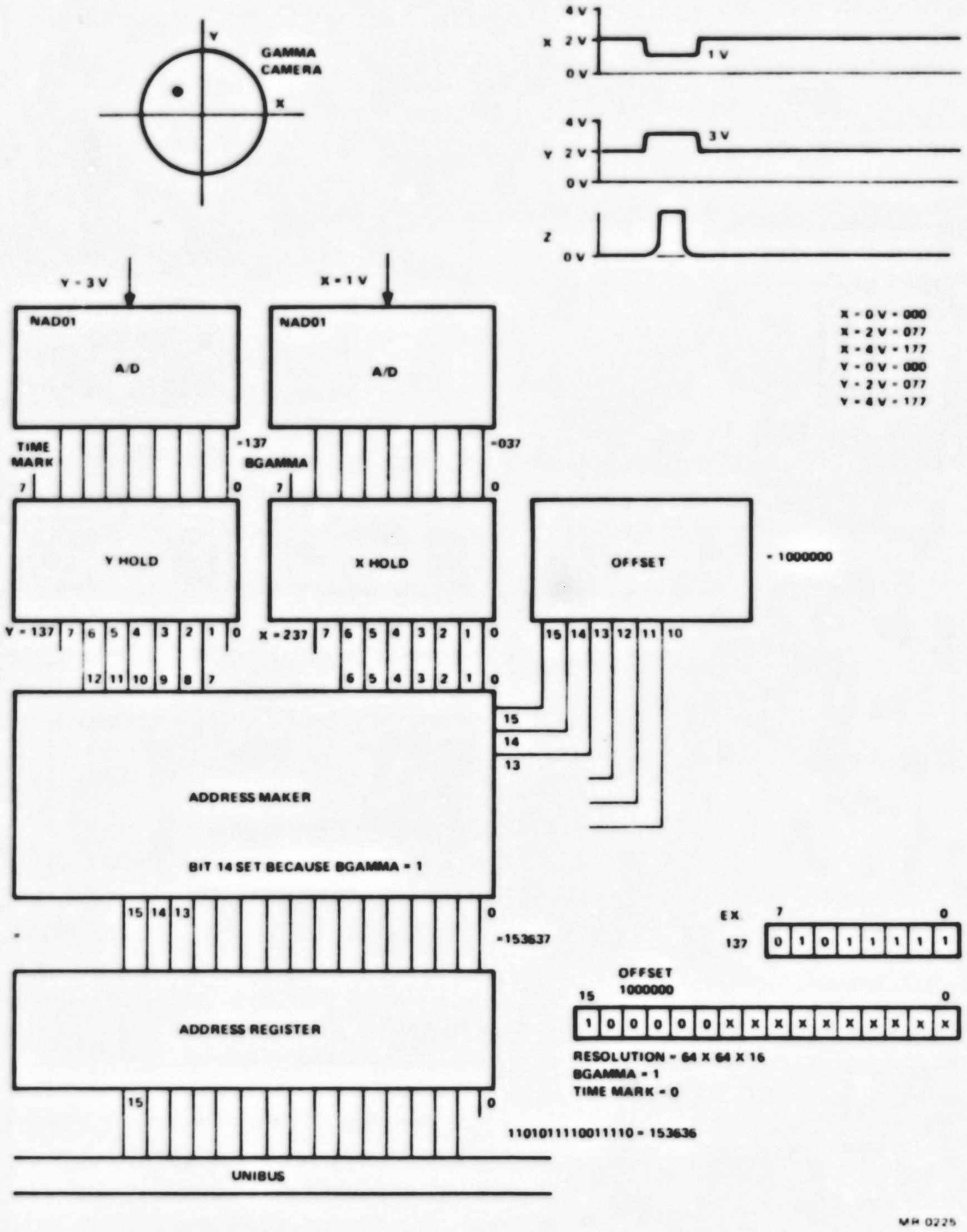

GAMMA CAMERA
Y
X
4 V
X 2 V
0 V
1 V
4 V
Y 2 V
0 V
3 V
Z
0 V
X = 0 V = 000
X = 2 V = 077
X = 4 V = 177
Y = 0 V = 000
Y = 2 V = 077
Y = 4 V = 177
Y = 3 V
X = 1 V
NAD01
A/D
NAD01
A/D
TIME MARK
=137
BGAMMA
=037
Y HOLD
X HOLD
OFFSET
= 1000000
Y = 137
X = 237
15 14 13 12 11 10
12 11 10 9 8 7
6 5 4 3 2 1 0
ADDRESS MAKER
BIT 14 SET BECAUSE BGAMMA = 1
=153637
ADDRESS REGISTER
UNIBUS
EX
137
0 1 0 1 1 1 1 1
OFFSET
1000000
1 0 0 0 0 0 X X X X X X X X X X
RESOLUTION = 64 X 64 X 16
BGAMMA = 1
TIME MARK = 0
1101011110011110 = 153636
MR 0225

Figure 5-3 Address Maker (example) (Sheet 2 of 2)

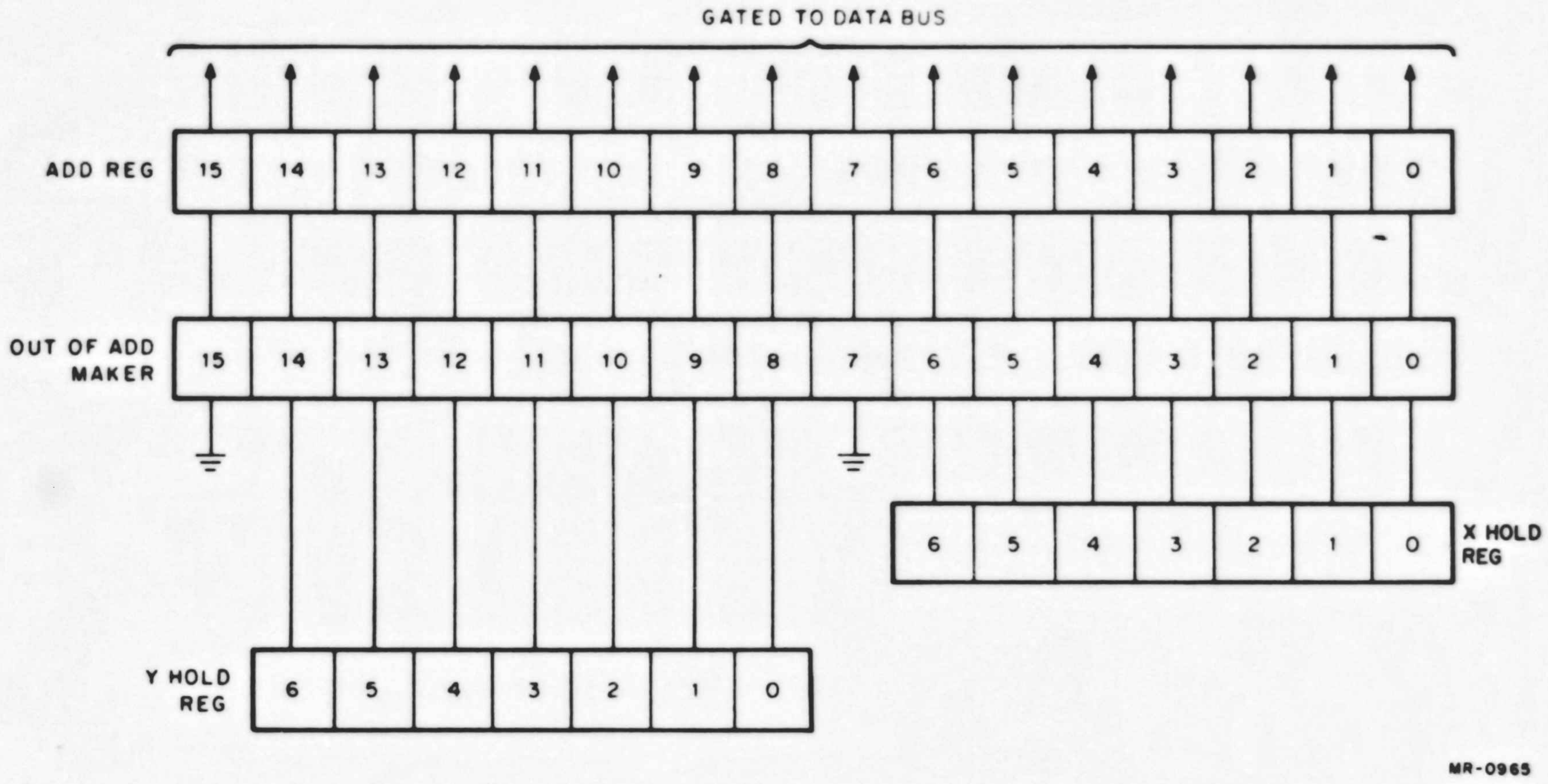

GATED TO DATA BUS
ADD REG
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
OUT OF ADD MAKER
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
X HOLD REG
6
5
4
3
2
1
0
Y HOLD REG
6
5
4
3
2
1
0
MR-0965

Figure 5-4 Joystick Address Maker

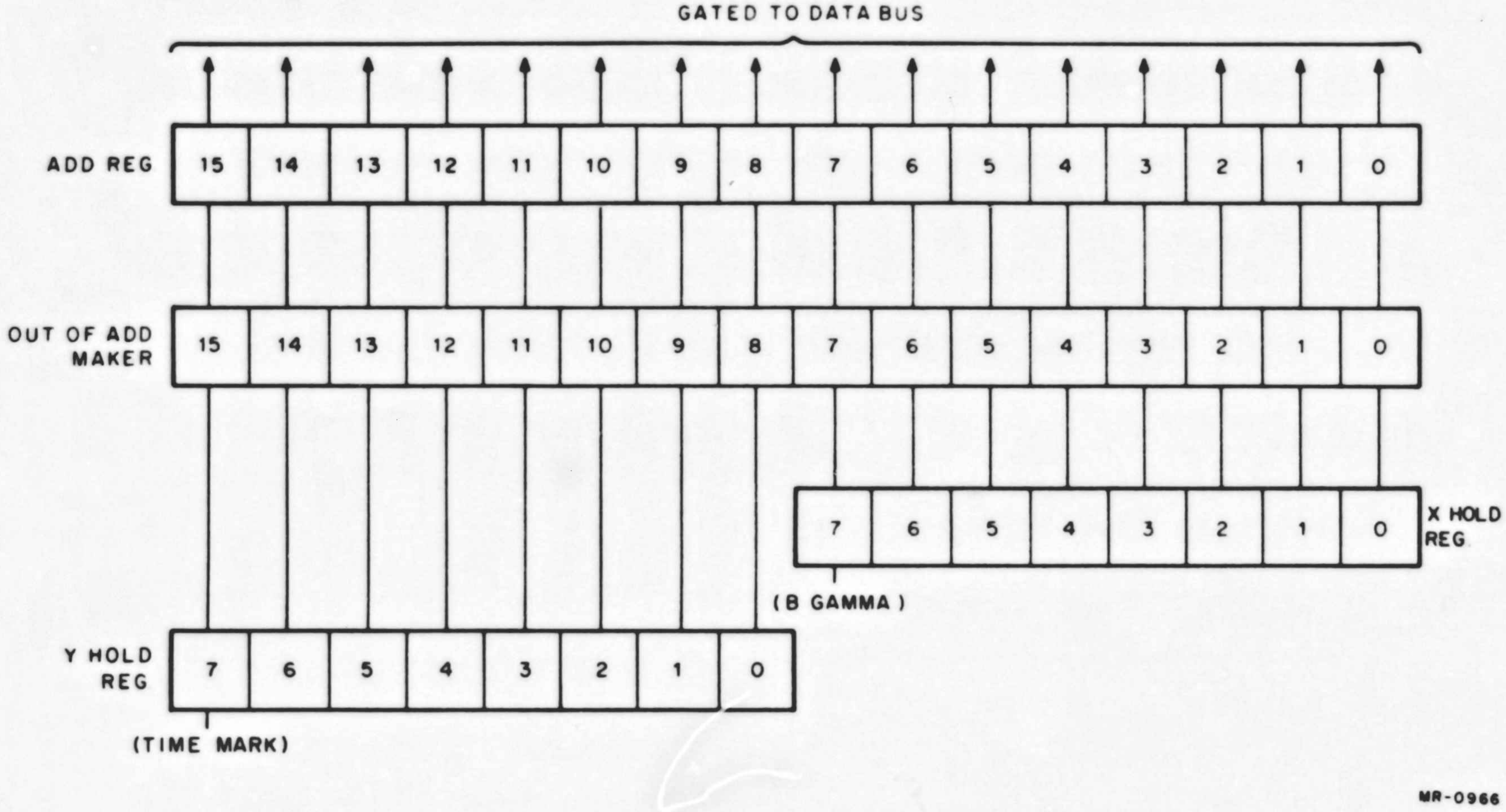
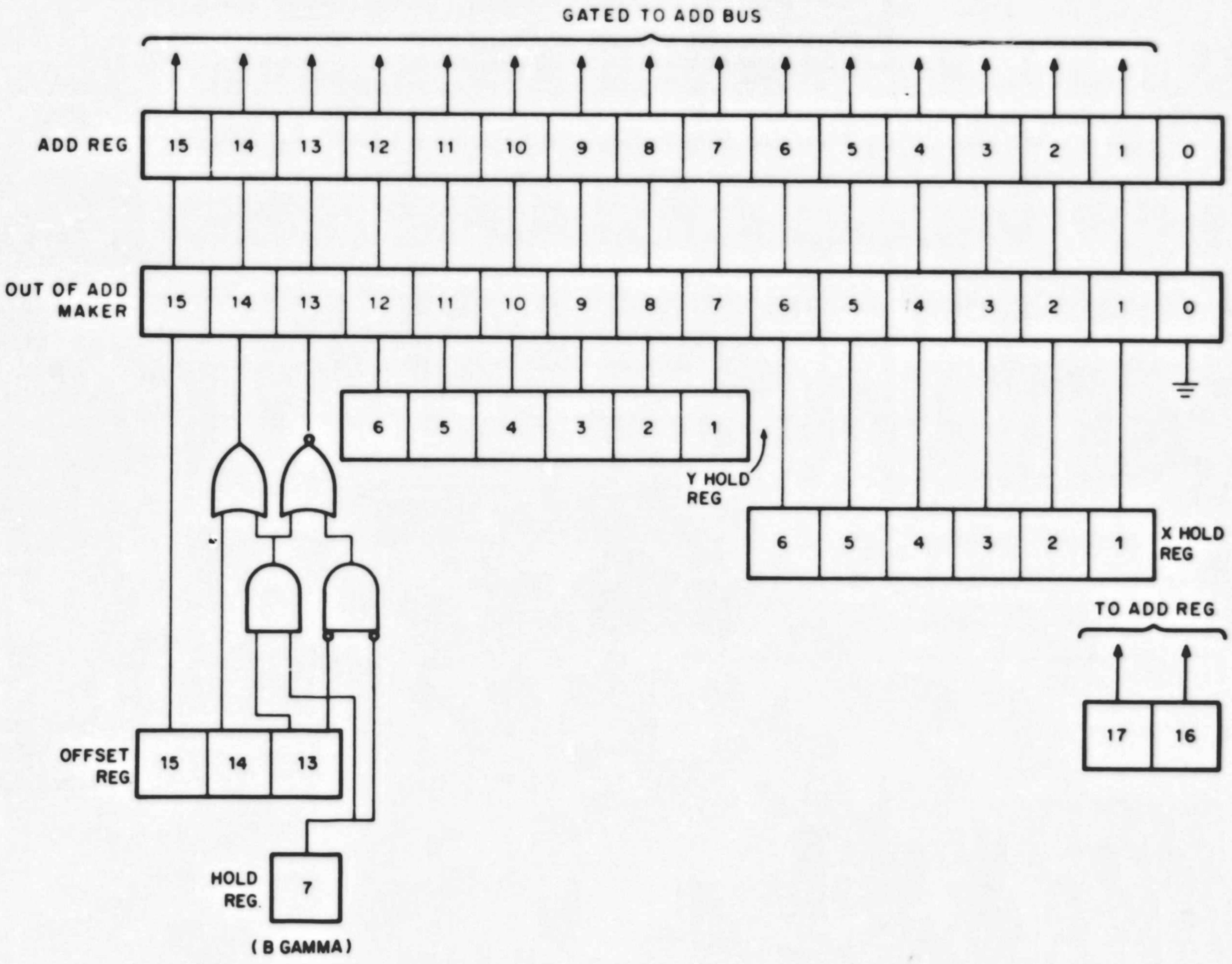

GATED TO DATA BUS
ADD REG
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
OUT OF ADD MAKER
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
X HOLD REG
7 6 5 4 3 2 1 0
(B GAMMA)
Y HOLD REG
7 6 5 4 3 2 1 0
(TIME MARK)
MR-0966

Figure 5-5 List Address Maker


GATED TO ADD BUS
ADD REG
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
OUT OF ADD MAKER
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
6
5
4
3
2
1
Y HOLD REG
6
5
4
3
2
1
X HOLD REG
TO ADD REG
17
16
OFFSET REG
15
14
13
HOLD REG.
7
(B GAMMA)

MR-0967

Figure 5-6 64 × 64 × 16 Matrix Address Maker

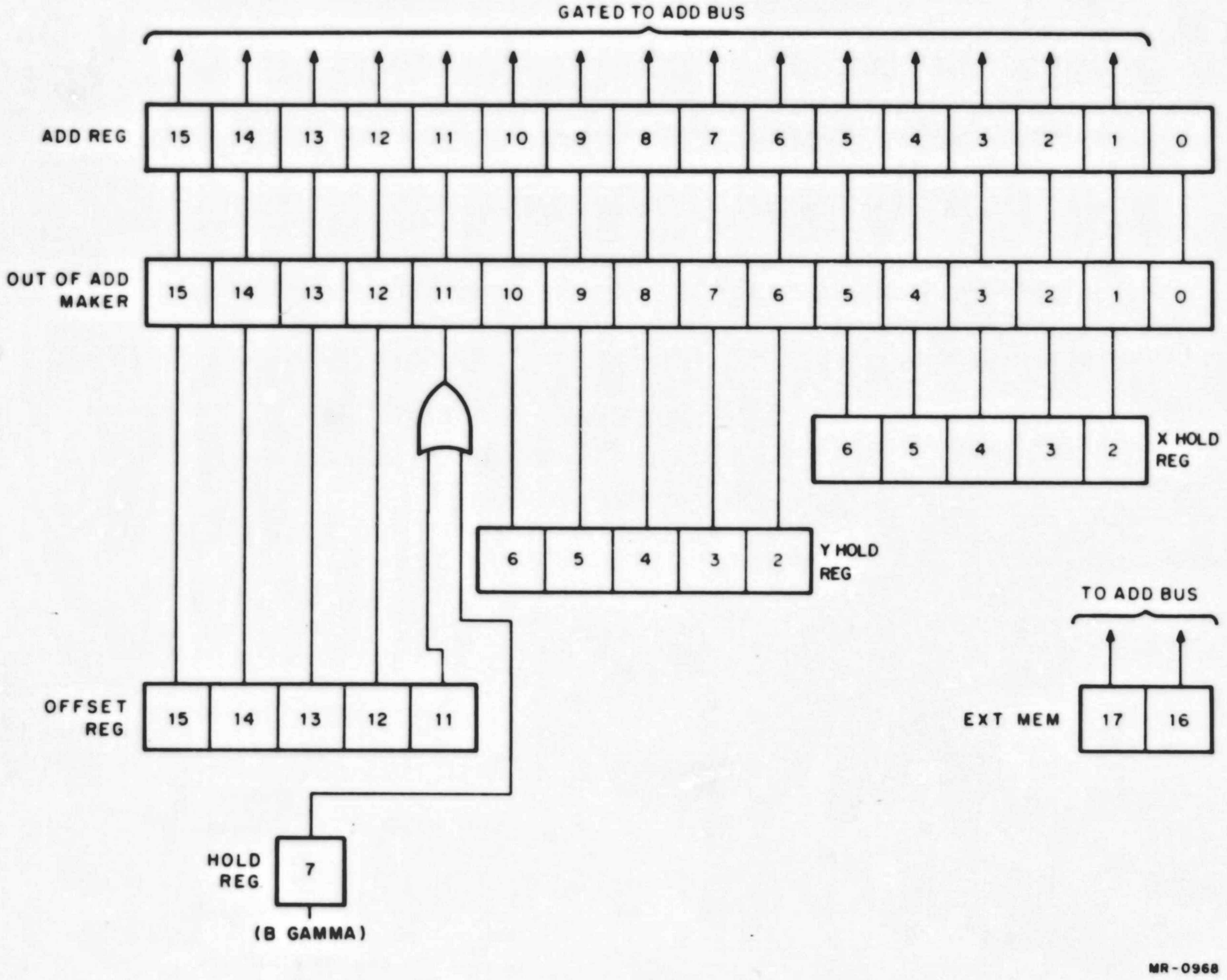

GATED TO ADD BUS
ADD REG
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
OUT OF ADD MAKER
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
6
5
4
3
2
X HOLD REG
6
5
4
3
2
Y HOLD REG
TO ADD BUS
OFFSET REG
15
14
13
12
11
EXT MEM
17
16
HOLD REG
7
(B GAMMA)
MR-0968

Figure 5-7 32 × 32 × 16 Matrix Address Maker

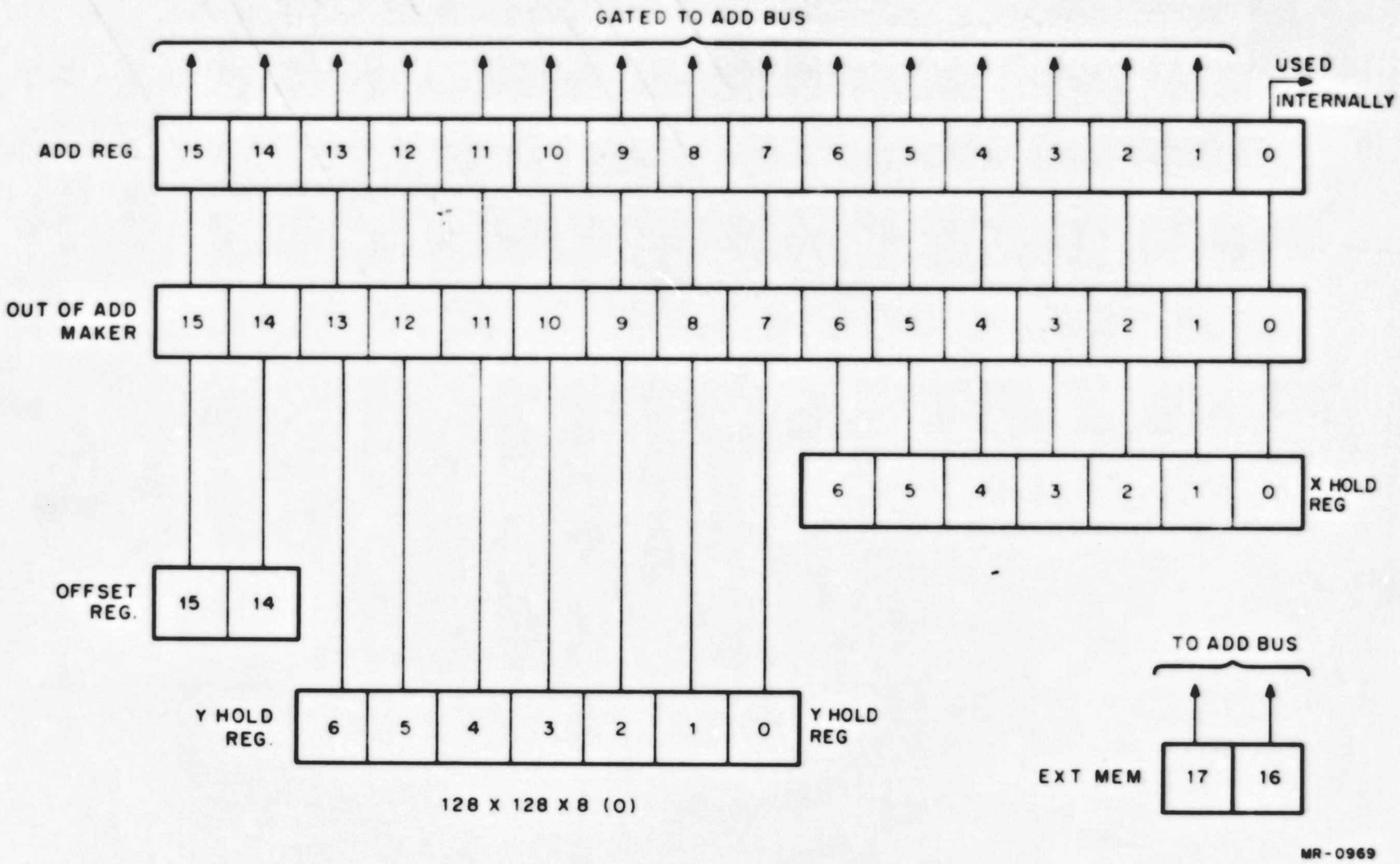

GATED TO ADD BUS
USED INTERNALLY
ADD REG
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
OUT OF ADD MAKER
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
6
5
4
3
2
1
0
X HOLD REG
OFFSET REG.
15
14
TO ADD BUS
Y HOLD REG.
6
5
4
3
2
1
0
Y HOLD REG
EXT MEM
17
16
128 X 128 X 8 (0)
MR-0969

Figure 5-8 128 × 128 × 8 (0K) Matrix Address Maker

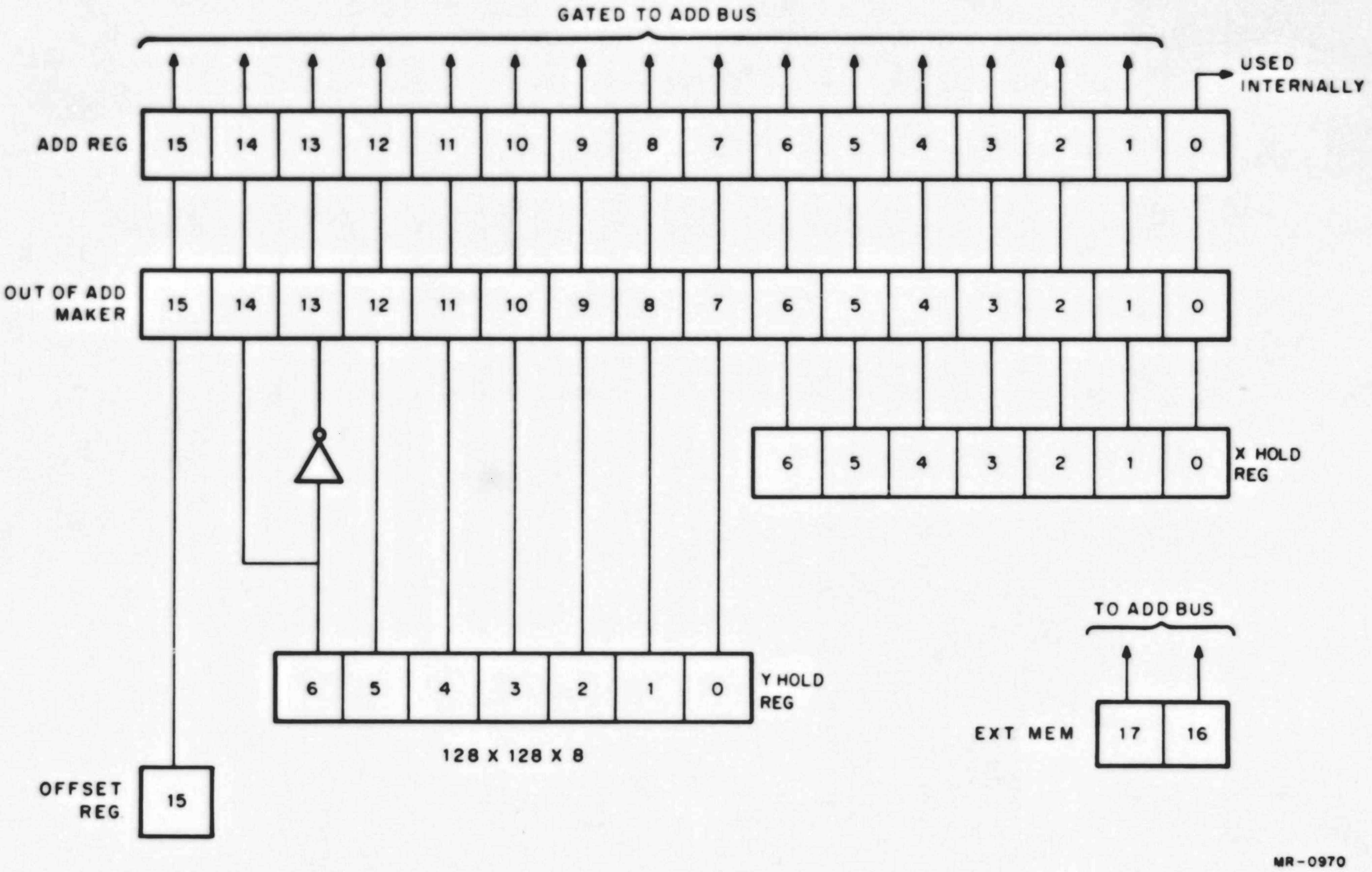
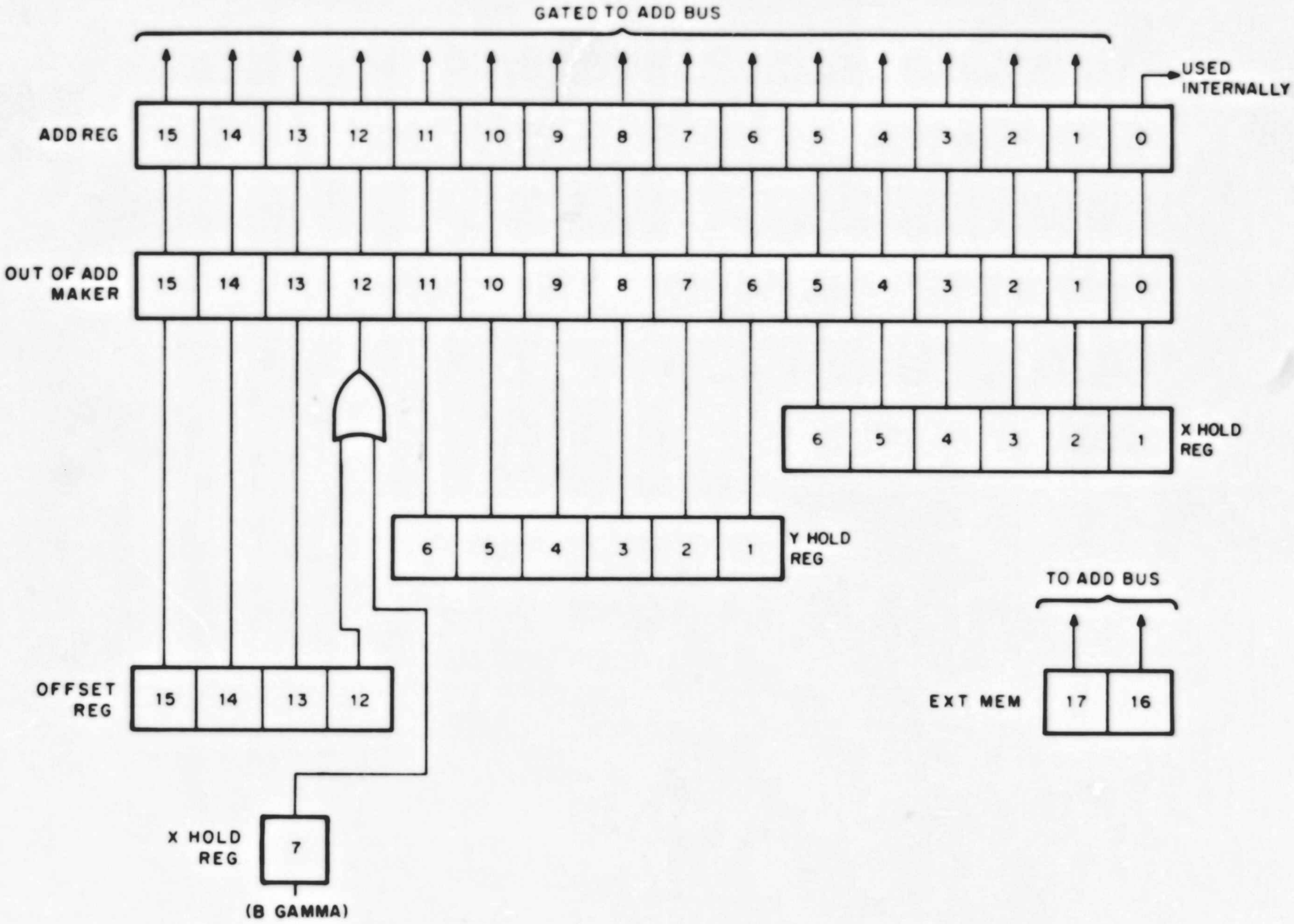
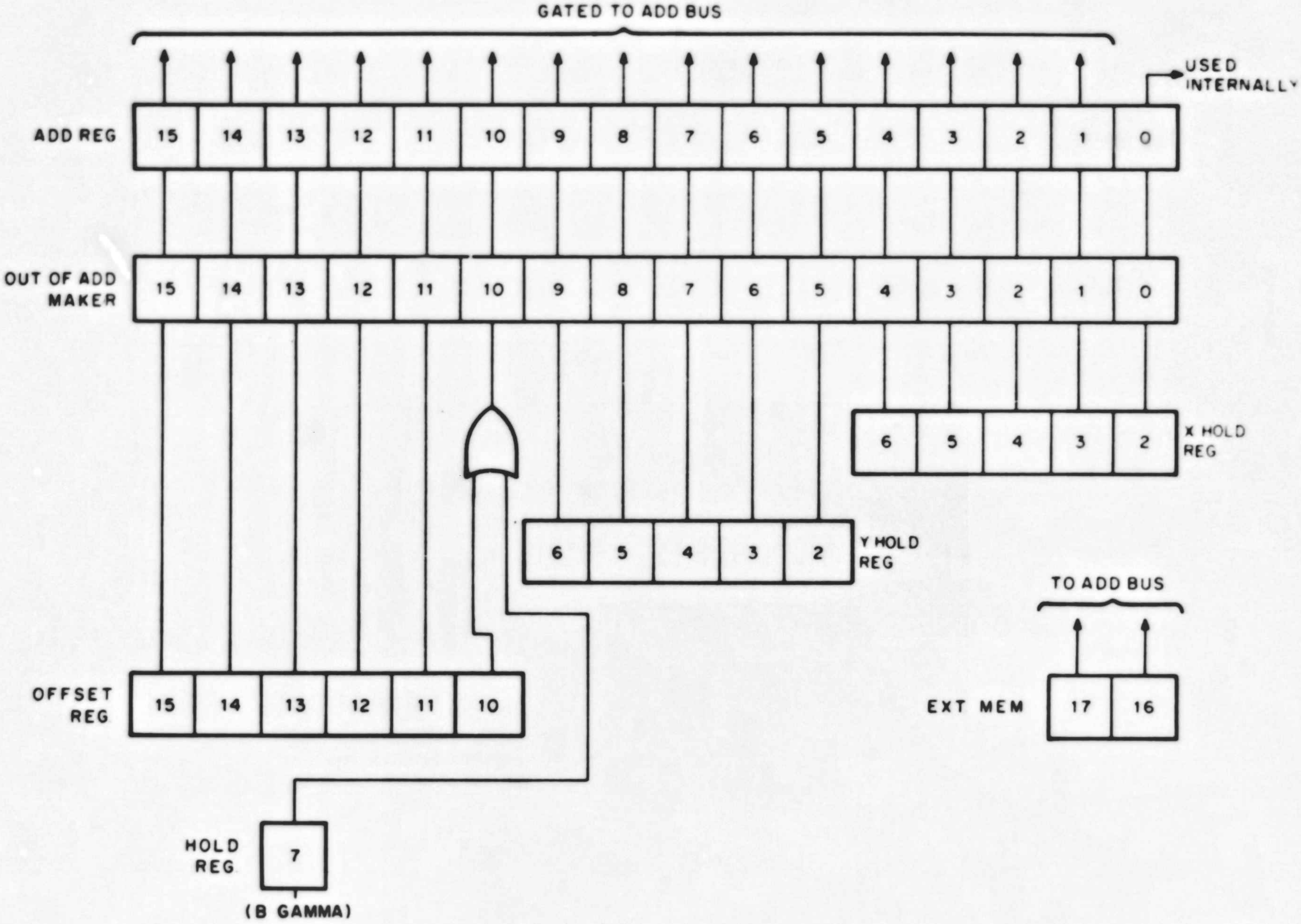

GATED TO ADD BUS
USED INTERNALLY
ADD REG
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
OUT OF ADD MAKER
X HOLD REG
Y HOLD REG
128 X 128 X 8
OFFSET REG
TO ADD BUS
EXT MEM
17
16
MR-0970

Figure 5-9 128 × 128 × 8 (4K) Matrix Address Maker


GATED TO ADD BUS
USED INTERNALLY
ADD REG
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
OUT OF ADD MAKER
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
X HOLD REG
6
5
4
3
2
1
Y HOLD REG
6
5
4
3
2
1
TO ADD BUS
OFFSET REG
15
14
13
12
EXT MEM
17
16
X HOLD REG
7
(B GAMMA)

MR-0971

Figure 5-10 64 × 64 × 8 Matrix Address Maker



GATED TO ADD BUS
USED INTERNALLY
ADD REG
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
OUT OF ADD MAKER
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
X HOLD REG
6
5
4
3
2
Y HOLD REG
6
5
4
3
2
TO ADD BUS
OFFSET REG
15
14
13
12
11
10
EXT MEM
17
16
HOLD REG
7
(B GAMMA)

MR-0972

Figure 5-11 32 × 32 × 8 Matrix Address Maker

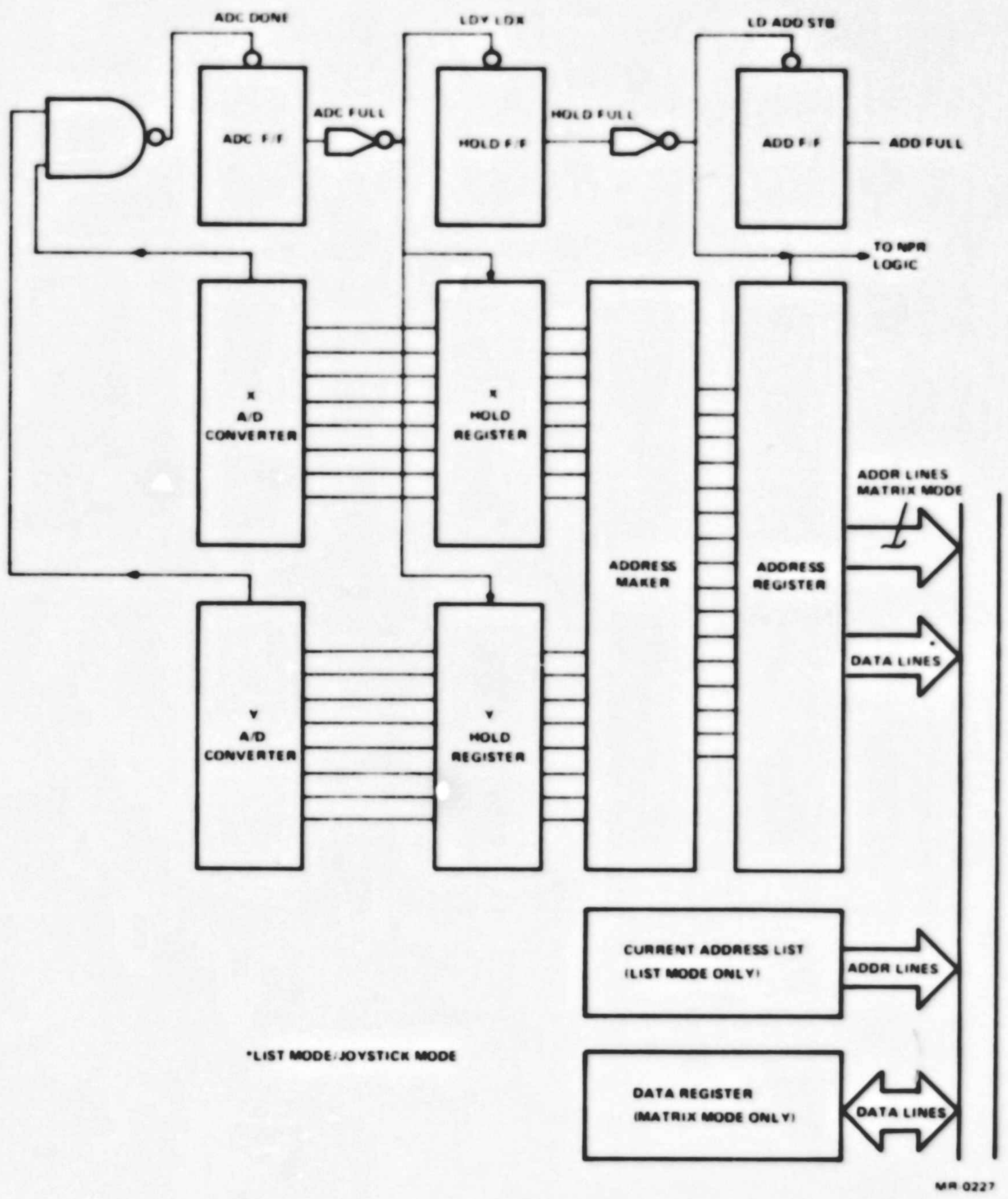

ADC DONE
LDY LDX
LD ADD STB
ADC FULL
ADC F/F
HOLD F/F
HOLD FULL
ADD F/F
ADD FULL
TO NPR LOGIC
X A/D CONVERTER
X HOLD REGISTER
ADDRESS MAKER
ADDRESS REGISTER
ADDR LINES MATRIX MODE
DATA LINES
Y A/D CONVERTER
Y HOLD REGISTER
CURRENT ADDRESS LIST (LIST MODE ONLY)
ADDR LINES
*LIST MODE/JOYSTICK MODE
DATA REGISTER (MATRIX MODE ONLY)
DATA LINES
MR 0227

Figure 5-12 Modes of Operation (Data Flow)

5.6 X AND Y HOLD REGISTERS (Drawing No. NC11-M-08)

The X and Y HOLD Register has two sources; direct input from the Unibus, and data from the A/D converters.

The direct input from the Unibus sets each flip-flop. Thus, all sixteen bits can be loaded in the register from the Unibus under program control.

NOTE

A test of the X-Y Hold Register via the Unibus does not test the "D" and "C" inputs to the register.

The data from the NAD01's converters provide the second source to the X-Y HOLD Register and includes the D09 TIME MARK and D09 B GAMMA signals. These inputs are clocked into the flip-flop by the D04 LD X and D04 LD Y signals. The flip-flops are cleared to a reset state by the D08 CLR X, Y HOLD signal from the Special Function Register (bit 00).

5.7 OFFSET WC, CA, Z REGISTERS (Drawing No. NC11-A-09)

The Offset, Current Address (CA), Word Count (WC), and Z Count Registers are shown in NC11-A-09. The upper portion of this drawing illustrates the Offset Register and B32 plug providing interconnection to the NAD01 converters. The logic shown in the lower portion are of the Word Count, Current Address, and Z Count Registers.

Data from the Unibus loads the Offset Register. The EXT MEM bits (00 and 01) are used when more than 32K of memory is required by the PDP-11. The higher order bits (10 through 15) are used by the Address Maker to provide offsets in memory.

The D09 TIME MARK flip-flop is set by D09 TM SNC signal. This signal is set by D10 SET TIME (bit 05) from the Special Function register under program control.

The 7-bit conversions from the X and Y A/D converters enter through connector B32. Also, entering B32 are the X and Y STORE signals which signify the completion of conversion, and the +12 V and -12 V which power the joystick (when connected). In addition, B32 provides the transfer of the D04 CLEAR ADC, D09 GAIN and D09 EXT signals from the NC11-A to the NAD01 converters.

The D04 CLEAR ADC resets the A/D converters to 0; the D09 GAIN and D09 EXT control the relays in the NAD01s. When the D09 GAIN is set (1) the NAD01s are forced into Zoom (gain 1); when reset (0) the NAD01 is placed in regular (gain 2). D09 EXT when set (1) will force the NAD01s to sample the EXT (Joystick) Input to the NAD01s. When reset (0), D09 EXT will force the NAD01s to sample Input 1 (signal from the Gamma Camera). EXT Input also provides connection of the H306 joystick when used in the system.

The Current Address (CA), Word Count (WC), and Z Count is a 32-bit register which functions differently in the List Mode and Matrix Mode. The 32 bits are split into two 16-bit registers when in the List Mode. One 16-bit register is the WC Register which is loaded with 2's complement of the number of list mode events to be registered. When this number is reached, an overflow occurs causing the NC11-A to interrupt. The WC Register is incremented by one for each Z pulse received from the Gamma Camera.

In the Matrix Mode, the 32-bit register is incremented by one for each Z pulse received from the Gamma Camera. In this mode, the operator can halt the NC11-A at a certain count by loading the 2's complements via the Unibus. When the predefined number of counts arrive, an overflow will be generated causing an interrupt.

5.8 ADDRESS SELECT SPECIAL FUNCTION (Drawing No NC11-A-10)

The logic for the Address Select and Special Function register operates in conjunction with the logic presented (in Drawing NC11-A-11) to control the communication with the Unibus. The base address (1640XX), for the NC11-A is set by the M105 which provides the logic necessary when an option is addressed on the Unibus. The M105 generates the D10 SEL, D10 OUT LOW, and D10 OUT HIGH when the base address is decoded. The M797 accepts these signals and decodes which NC11-A register is selected. The D10 OUT LOW and D10 OUT HIGH signals are derived from address bit A00 and bits C0 and C1 from the Unibus. Table 5-4 lists a summary of registers including addresses, directions and functions.

Table 5-4 Register Summary

Address	Direction	Register Type
164000_8	Destination	Load Command register.
	Source	Read Command/Status register.
164002_8	Destination	Load Offset register.
	Source	Read Offset register.
164004_8	Destination	Load X-Y register.
	Source	Read Address register.
164006_8	Destination	List Mode: Load Word Count. Matrix mode: Load High Z.
	Source	List Mode: Read Word Count. Matrix mode: Read High Z.
164010_8	Destination	List Mode: Load Current Address Matrix mode: Load Low Z.
	Source	List Mode: Read Current Address Matrix mode: Read Low Z.
164012_8	Destination	Load Increment register.
	Source	Read Increment register.
164014_8	Destination	Special functions
	Source	Not used

A group of gates produce the Special Function Register which may be set under program control to produce seven control functions (see Table 5-5).

Bit 02 allows the programmer to force an A/D conversion in the NAD01s. Bit 03 clears Joystick DEP Flag which is set either by the joystick interrupt bar on the H306 joystick (if connected to the NC11-A) or by depressing the Remote Start switch.

The standard Gamma-11 software can set-up a programmable clock to interrupt every 10 ms, advancing the program to a section where bit 05 of the Special Function Register is set; which sets the D09 TIME MARK flip-flop. The next time converter information from the NAD01s are transferred to the X and Y Hold Registers, bit 15 will be set. When a study is played back, the software program can keep track of the Time Marks.

Table 5-5 Special Function Register

Bits	Control Functions
Bit 00	Clears the X,Y Hold Register
Bit 01	Clears the INCR OVFL Flag
Bit 02	Software conversion pulse
Bit 03	Clears the Joystick DEP Flag
Bit 04	Clears the Z/WC overflow, WC, and CA Registers
Bit 05	Sets TIME MARK Flag
Bit 06	Resets the NC11-A and NAD01s

This function allows the operator to control the timing of data which produces a picture from a study; for example, if each picture of a study has one second of data, the program will count one hundred Time Marks and use that data for a picture.

NOTE

It is necessary to set bit 06 two times. (Special Function Register). This is required to compensate for transactions which may take place during the reset cycle.

5.9 NONPROCESSOR REQUEST (NPR) CONTROL LOGIC (Drawing No. NC11-A-11)

Two M7821s (slots B06 and B07) operate in conjunction with the M796 (slot B08) to provide control of the Unibus for interrupts and NPR cycles.

5.9.1 Interrupt Control

Two events cause an interrupt in the NC11; Increment Overflow, and Z/WC overflow which Vector to 270 and 274 respectively.

NOTE

Only the M7821 in Slot B06 is used for interrupts.

Signal D03 INT (1) H causes the M7821 to assert BUS REQ L. On receipt of BG IN H, it asserts SACK L, BUS INTR and the appropriate vector address. INTR DONE clears the INT flip-flop.

5.9.2 NPR Control

In the Matrix mode, both M7821 modules are utilized. The M7821 in Slot B06 has priority over the M7821 in slot B07: i.e., the NPG Grant Signal connects first to the M7821 in slot B06. The LD ADD STB signal causes both REQ RW H (coordinate C,4) and REQ NPR (coordinate B,4) which sets flip-flops READ (1) H and FIRST NPR (1) H, respectively. Signal READ (1) H going true sets REQ R (1) (read cycle) which requests an NPR cycle via the M7821 (Slot B06). The READ (1) L signals also sets RS flip-flop REQ W (1) H (coordinate B,2) which posts an NPR request through M7821 (Slot B07). The M7821 (Slot B06) will assert BUS SACK and then MASTER R as soon as B BSY goes high.

Signal MASTER R is gated to the M796 Unibus control module (slot B08). MASTER R and READ (1) initiate a DATI cycle, gating the Address Register to the Address bus with the ADD TO BUS signal (coordinates D,4). The M796 sets BUS MSYN and waits for the slave to respond with BUS SSYN. Upon receipt of BUS SSYN the M796 generates DATA WAIT H which is used to load the Data Register with the content of the Bus Data lines. DATA WAIT causes DATA STROBE (coordinates B7) which is used to increment the data register, cancels MSYN and generates RIP DEL. END cycle occurs at the end of DATA STROBE and is used to clear the READ flip-flop, the REQ R flip-flop, and the FIRST NPR flip-flop. The NPR logic still has REQ W (1) flip-flop set to request the second NPR (write cycle).

The RIP DELAY of 400 ns is used to allow time for the Data Register to increment and if an overflow occurs set the INCR OVFL flip-flop. RIP DELAY also is used to inhibit MASTER W from gaining bus control until INCR OVFL flip-flop is set in the case of overflow. If an overflow occurs the trailing edge of RIP DEL triggers the M606 pulse amplifier (coordinates B5) which resets the REQ W flip-flop and cancels the second NPR cycle. If overflow does not occur the second NPR cycle is initiated upon receipt of bus NPG IN. Note that a higher priority NPR device can be granted a cycle between the read and write cycles of the NC11.

MASTER W and READ (0) are used by the M796 to control the bus for a dato cycle. The M796 will assert bus C1, ADD TO BUS, and DATA TO BUS. DATA TO BUS "ANDed" with LIST MODE (0) asserts RD I REG (coordinates C, 4) which gates the Data Register that has just been incremented to the Data lines. The Address Register is gated to the Address lines by ADD TO BUS. The M796 then asserts MSYN and waits for the memory to respond with SSYN. When SSYN is received, the M796 generates END CYCLE which clears the REQ W flip-flop via NAND GATE M113, B16 (coordinates B, 4) and relinquishes control of the bus.

NOTE

NPR DONE which goes to the control logic is not generated until the end of the second NPR.

In the list mode, only one NPR cycle is performed for each conversion. The signal SET REQ is used to clear the READ flip-flop and SET the REQ R flip-flop to request an NPR cycle.

NOTE

Although the cycle is a DATO the request is via the M7821 in location B06.

Upon gaining control of the bus the M796 gates the CA Register to the Address lines via the signal CA TO A BUS (coordinates D, 5) and gates data from the Address Register to the data line via the signal RD ADD REG (coordinates C, 3). RD ADD REG is a direct result of LIST MODE (1) "ANDed" with DATA TO BUS H (coordinates C, 5). The M796 asserts MSYN and waits for a SSYN from the memory. SSYN causes the M796 to clear MSYN and issue END CYCLE which clears the REQ R flip-flop ending the NPR cycle. The process continues until Word Count overflows.

5.10 COMMAND AND DATA REGISTER GATING TO BUS (Drawing No. NC11-A-12)

The Command and Data Register Gating to Bus consists of two groups of gates which functions as a 2 × 1 multiplexer. The gates receive data from the Command and Status Register or Data Register and are gated into the internal U bus. The U bus is transferred to the Unibus through drive circuitry depicted in Drawing No NC11-A-15.

5.11 ADDRESS AND OFFSET GATING TO BUS (Drawing No. NC11-A-13)

The two groups of gates transfers data from the Address Register or Offset Register to the Unibus Data lines through driver circuits shown in NC11-A-15. Only one register can be selected at a time.

5.12 ADDRESS REGISTER OUTPUT GATING DRIVER (Drawing No. NC11-A-14)

This register contains two groups of gates which receives data from the Address Register and gates that information onto the Unibus Address line.